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THE SNYTHESIS OF AN MTI CANCELLATION FILTER USING CAPACITIVE STORAGE ELEMENTS IN THE DELAY LINE

by

Robert Lee Peterson

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THESIS

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The Synthesis of an MTI Cancellation Filter Using Capacitive Storage Elements in the Delay Line

by

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Lieutenant(junior grade), United States Navy
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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

By using a series of diode sampling gates and capacitive storage elements to achieve the necessary time delay, a cancellation filter is designed that will give a maximally flat passband and that will give subclutter rejection at zero frequency and at harmonics of the pulse repetition frequency. Such a filter is necessary in each range channel of moving target indication (MTI) radar systems. Theoretical results obtained from digital simulation are compared with actual results obtained upon completion of the filter synthesis, and a brief evaluation of the entire range channel is presented.

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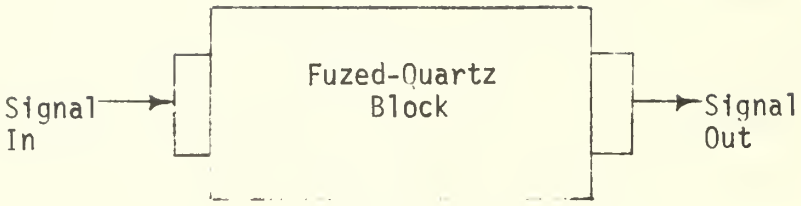
I. INTRODUCTION

The increased emphasis upon reducing size, weight and cost of components, coupled with the recent rise of integrated circuits as an efficient and reliable method of achieving the above three goals has paved the way for the revision of existing construction methods. With existing technology, MTI type radars presently use cancellation filters which involve the use of quartz or mercury delay lines. A typical quartz delay line is represented in Figure 1. The length of the time delay is proportional to the total acoustic path length, and hence to the number of times the signal is reflected from the facets or sides in the fuzed quartz block of the delay line.

A typical delay line itself weighs ten to fifteen pounds, and the actual package is twelve to eighteen inches in diameter and about one and one half inches thick. The cost of such a delay line ranges from several hundred to several thousand dollars. Thus if it were possible to perform the function of the delay line on integrated circuit chips, size, weight, and cost reduction could all be achieved, with the additional benefits of greater efficiency and much improved reliability. These chips could then be incorporated into an MTI radar, thereby achieving the desired goals of reduced size, weight and cost.

The use of MTI radar systems is important for discerning moving targets in the presence of fixed targets whose undesired radar returns may be much stronger than those of the moving targets. MTI operation



Basic type fuzed-quartz delay line

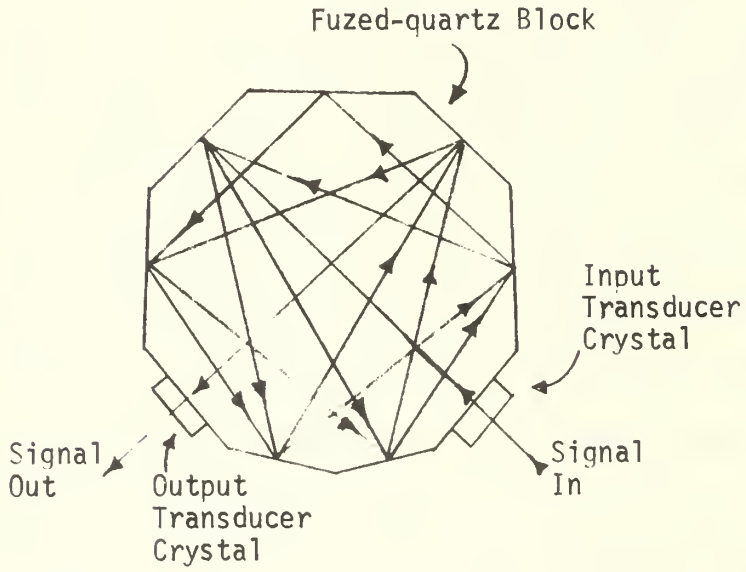


Fig. 1. Quartz delay line

is based on the fact that moving targets create a doppler frequency shift which is proportional to the radial component of velocity at which the target moves. Strong fixed target returns may camouflage weaker moving target returns, and therefore a cancellation filter which rejects these fixed echoes is necessary.

Present use of quartz or mercury delay lines in the cancellation filters of MTI systems gives moving target range information which is continuous. Thus, if any part of the filter is inoperable, the entire system ceases to function. If the range information were obtained from the composite output of a number of parallel range channels, one for each range, then even if one of the channels was inoperable, the majority of the information would still be available. Figure 2 indicates one of the necessary range channels of such a system. In addition to increasing the overall reliability of the system, the narrow range intervals allow for narrow band filtering without destroying any important range information. Timing circuits allow the bi-polar video input to be sampled in turn for successive range channels and then to be reconstructed at the output of the range channels.

The cancellation filter is discussed in the following chapters of this thesis, and the rest of the range channel is discussed in the thesis of E. L. Washam [Ref. 1].

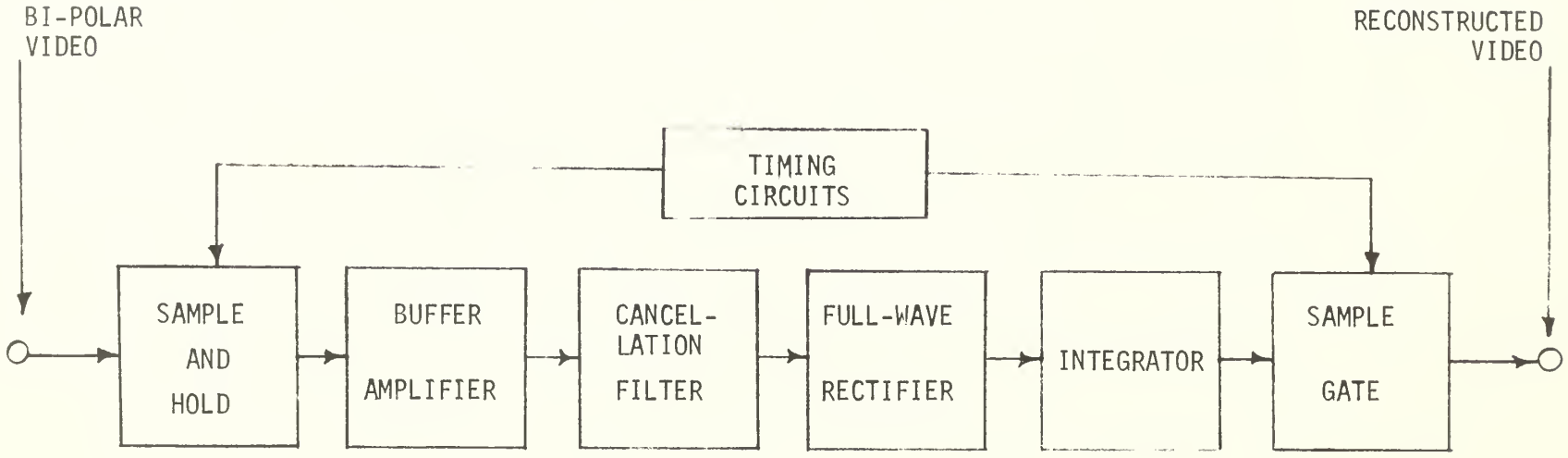


Fig. 2. Typical range channel

II. DESIGNING A CIRCUIT

In a paper by Warren D. White [Ref. 2], a transfer function, H(z), which gives the desired maximally flat passband and rejection of harmonics of the pulse repetition frequency is suggested. He indicates that the transfer function,

$$H(z) = \frac{(z-1)^3}{(z-.04)(z^2-.88z + .61)} , \qquad (1)$$

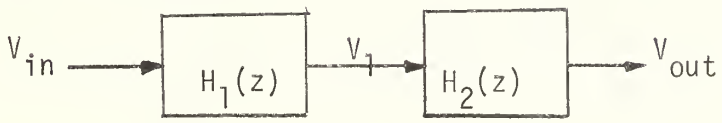
could best be synthesized in two parts; the first,

$$H_1(z) = \frac{z-1}{z-.04} , \qquad (2)$$

and the second,

$$H_2(z) = \frac{(z-1)^2}{z^2 - .88z + .61} \qquad (3)$$

In the above equations, $z = e^{j\omega T}$, where T is the reciprocal of the pulse repetition frequency. In block diagram form equations (1), (2), and (3) may be reduced to



In his book, Merrill I. Skolnik [Ref. 3] elaborates upon this block diagram, as seen in Figure 3 below.

The derivations of the transfer functions from Skolnik's block diagram are shown in Appendix A.

By simulating these block diagrams on the digital computer, frequency responses for the first stage, second stage, and complete circuit may be obtained. The computed data points from the simulated

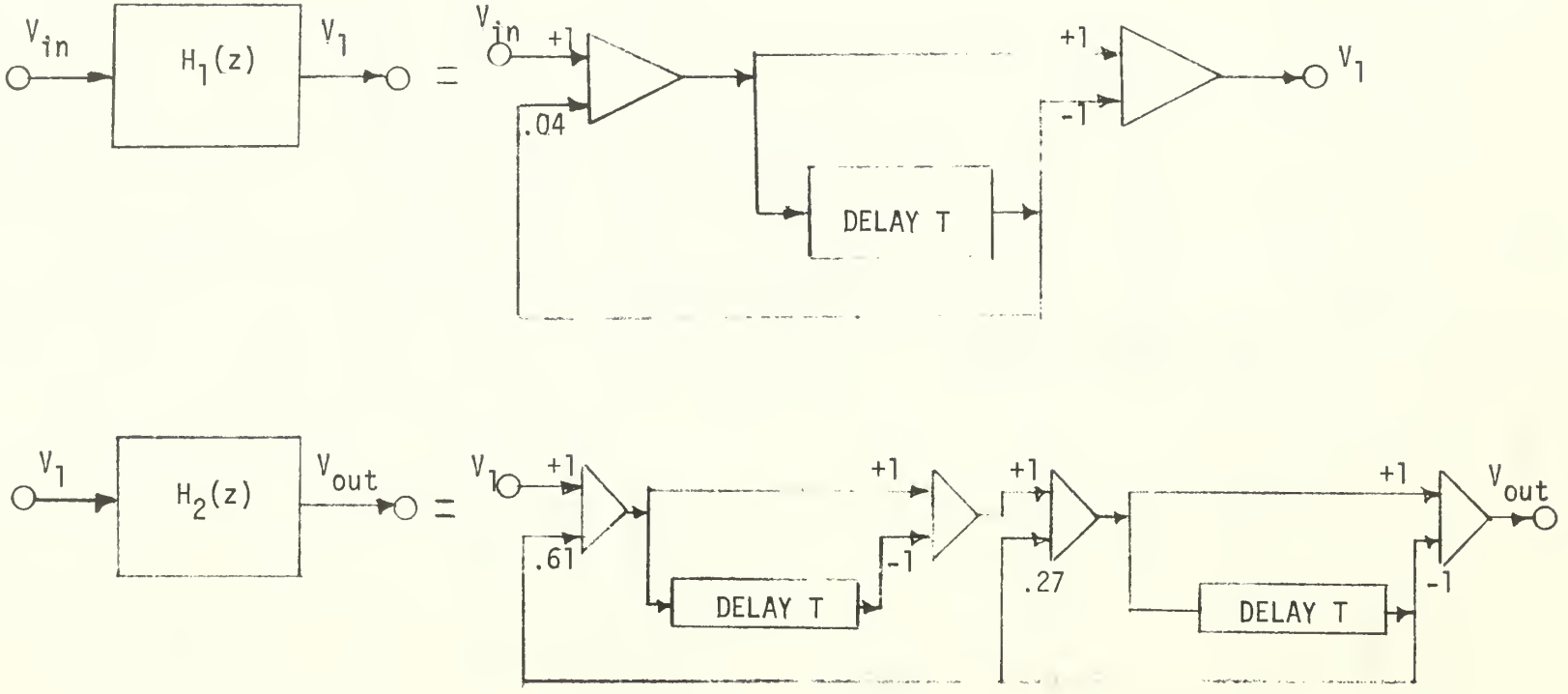


Fig. 3. Block diagrams of $H_1(z)$ and $H_2(z)$

system and corresponding frequency responses are shown in Appendix B. The response of stage one closely duplicates that of the positive portion of a sine wave which is shown in dashed lines on the first stage response. The effect of the small feedback factor is to bulge the frequency response somewhat. Once a working model of the filter is built, these responses will provide a basis for determining if the filter actually satisfies the requirements of the system.

The theoretical characteristics of this filter can be compared with those of simple RC differentiating filters of one, two and three stages and two cases of an integrator-summer circuit presented by Mitchell [Ref. 4]. The comparison shown in Figures 4a and 4b indicates that the cancellation filter gives the best combination of clutter rejection at zero frequency and maximum gain in the passband.

In order to synthesize such a filter, at least two decisions must be made. The first is to decide how to accomplish the required additions, and the second, and more complicated is to decide how to achieve the desired delay. For the AN/UPS-1, the pulse repetition frequency is 800 cycles per second, and the required delay is therefore 1.25 msec.

The problem of addition is easily solved by a form of collector summation. By having the voltages to be summed at the collectors of two separate transistors, addition may be obtained by applying these voltages to the top and bottom of a voltage divider. The center tap output will then be proportional to the sum of the two inputs. If the resistors are made equal, the output will equal one half of the

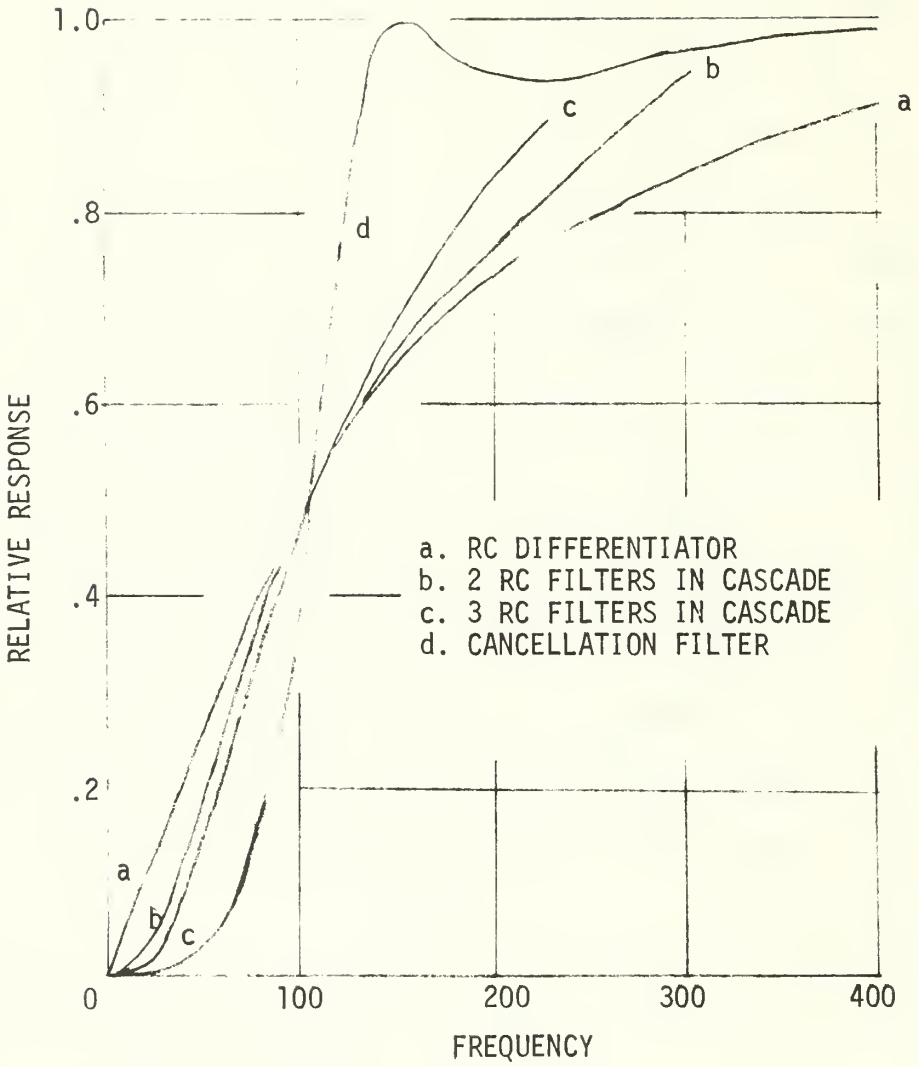


Fig. 4a. Response comparison

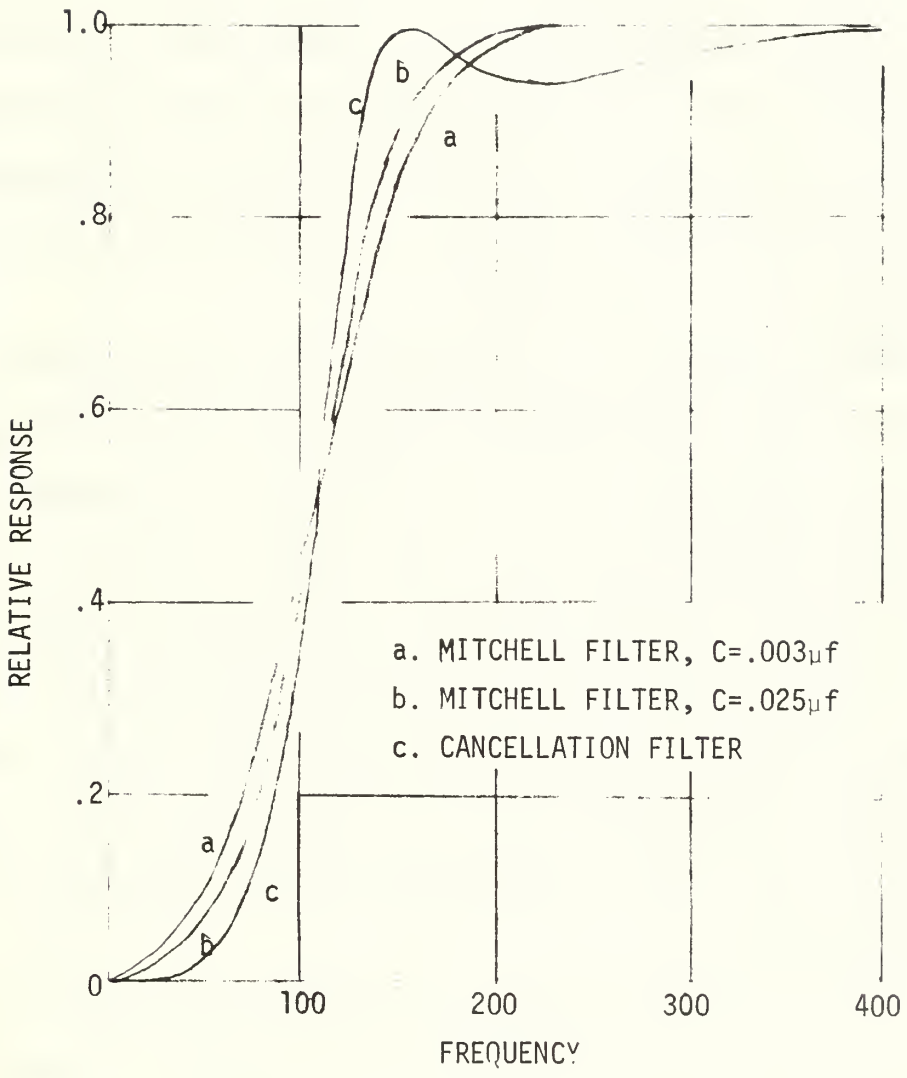

1.0
.8
.6
.4
.2
0
RELATIVE RESPONSE
100
200
300
400
FREQUENCY
a
b
c
a. MITCHELL FILTER, C=.003μf
b. MITCHELL FILTER, C=.025μf
c. CANCELLATION FILTER

Fig. 4b.

sum of the inputs, as seen in Figure 5 below. An amplifier stage may then be used to recover the voltage lost in the addition process.

One method of accomplishing the 1.25 msec delay is by the use of an artificial transmission line. However, delays of this magnitude would require either the use of a tremendous number of stages or the use of fewer stages containing unreasonable values of inductance. In addition, integrated circuit design favors the use of capacitors and resistors rather than inductors. Thus, the use of an artificial transmission line is impractical.

Another possibility, which proves to be feasible, involves the use of a sampling circuit and a series of switches each followed by a storage capacitor in which the signal component is stored for the required length of time, which in this case is 1.25 msec. The sampling circuit and the switches can be triggered by pulses separated in time by 1.25 msec. The value of the storage capacitor should be made small enough to give a fast charging time constant. It must, however, be large enough so that the input voltage level is maintained for the entire 1.25 msec with a minimum of droop due to discharge by leakage.

If the sampler and switches are gated on by the same set of trigger pulses, they will all be on simultaneously. Therefore, a fraction of the same sample voltage, depending upon the ratio of the capacitors, will appear on all storage elements, and no delay will take place.

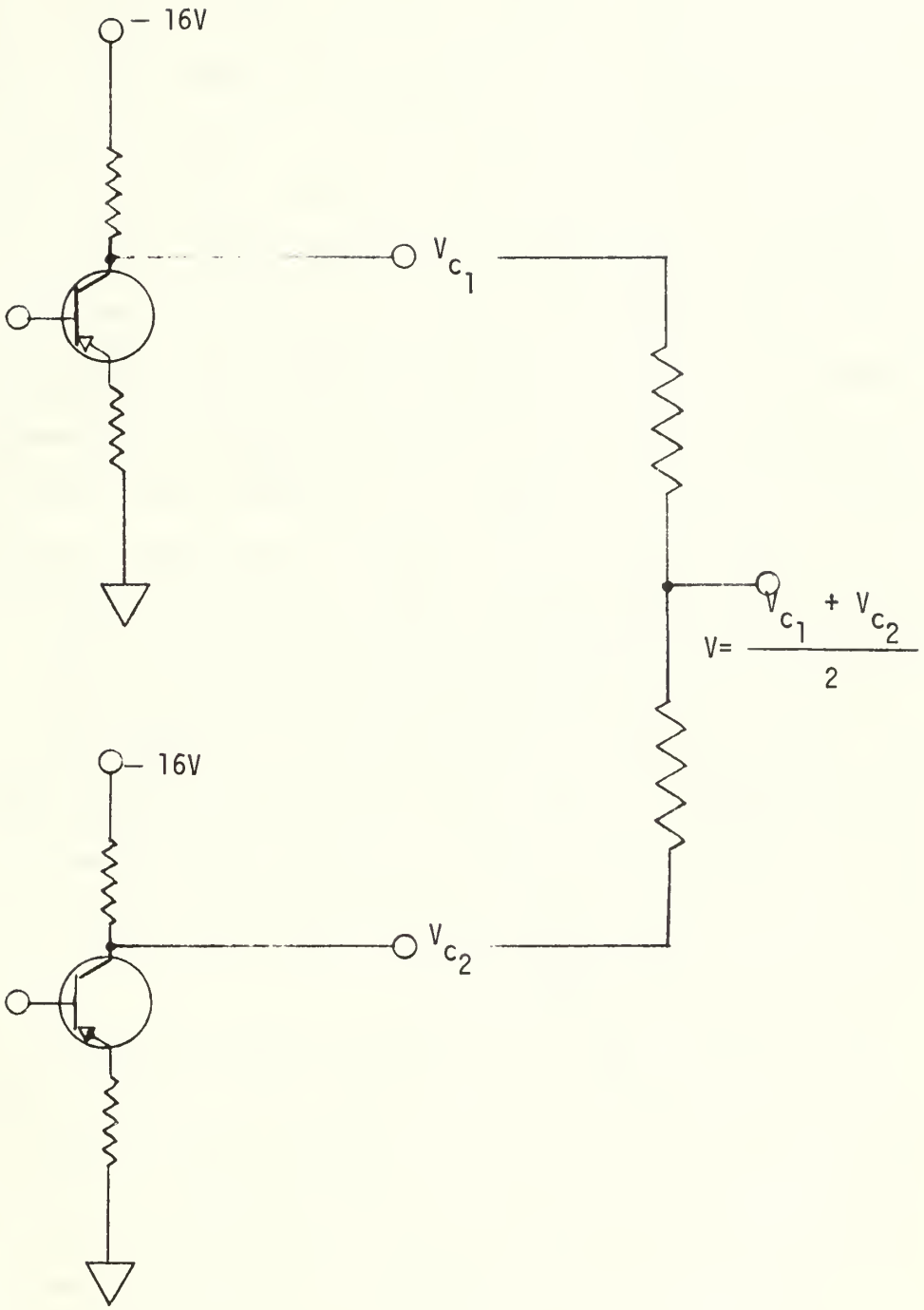


Fig. 5. Summing circuit

If, however, the switch following the sampling circuit is gated on by a pulse between basic range pulses occurring every 1.25 msec, then the delay can be achieved as indicated in Figure 6. This first switch can be triggered during the period when the sampler and second switch are gated off. For example, if the trigger pulses for the sampling circuit and the second switch are 100 μsec in duration, then these elements are gated off for 1.15 msec. If the first switch is triggered at any point within this interval, then a capacitive ratio of the original sample value voltage will appear at the storage element of this switch. When the original trigger pulse gates on the sampling circuit and the second switch again, a new sample value appears at the storage element of the sampling circuit and a fraction of the original sample voltage appears at the storage element of the second switch. Amplification stages are necessary to recover the voltage lost when the sampler and the switches are gated on. The amplified output at the storage element of the second switch is now delayed 1.25 msec from the sample voltage at the output of the sampling circuit. These sample voltages may now be added with opposite polarity in order to achieve the delay cancellation required in the block diagram of Figure 3.

The delayed trigger pulses mentioned above may be easily obtained by triggering a monostable multivibrator with the trailing edge of the trigger pulse used both on the sampling circuit and the second switch. By differentiating the positive trigger pulse, two spikes are obtained. The positive spike may be eliminated by the use of a diode in parallel with the resistor in the differentiating circuit

as shown in Figure 7. This negative spike is delayed by the width of the triggering pulse, and when it is applied to the monostable multivibrator it yields a positive delayed pulse at the collector of one transistor and a negative delayed pulse at the collector of the other. The width of these pulses is determined by the time constant built into the multivibrator.

The respective feedback factors may be obtained by attenuation of the output of the proper delay circuitry in accordance with Figure 3. These voltages may be added to the input of the delay circuitry by the method shown in Figure 5. Feedback oscillation is not an important consideration here since the feedback factors are less than unity.

If the sampler and switch circuits are chosen properly, this form of delay line will lend itself well to integrated circuit conversion. If, for example, an electromechanical chopper were to be used for either the sampler or the switch, this adaptability would be lost. While the electromechanical chopper is an ideal switch in that it is characterized by extremely high off impedance in the order of thousands of megohms and a very low on impedance of milliohms, it is relatively slow and bulky and would not convert readily to integrated circuit design.

The simplest type of sampler or switch is the solid-state-diode bridge. The diode bridge is extremely economical and is faster than the electromechanical types. Diode bridges are best suited for signals in excess of 100 mV, and since the input to this circuit will be typically five to ten times that amount, it is

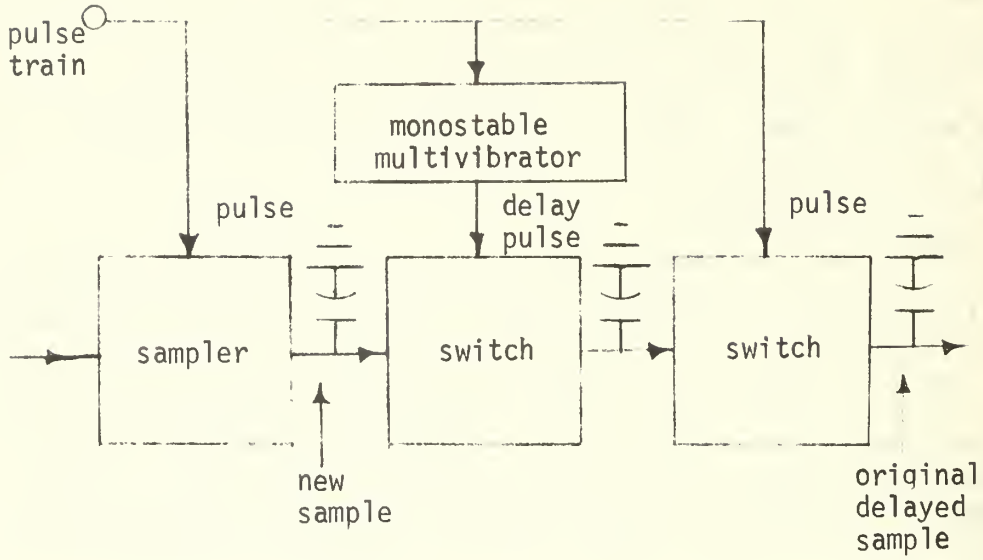


Fig. 6. Delay schematic

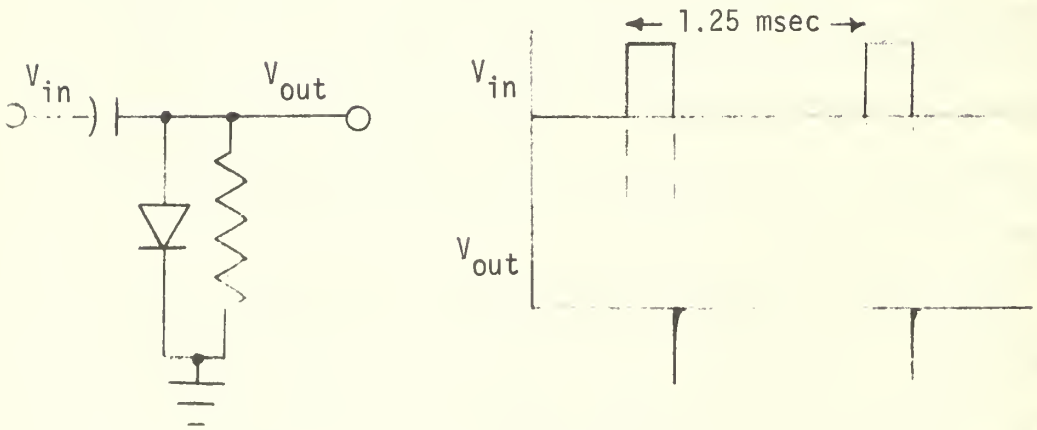


Fig. 7. Differentiating circuit with input and output

ideally suited for this application. Although not as good in this respect as is the electromechanical chopper, the diode bridge also has an extremely high off impedance and a low on impedance.

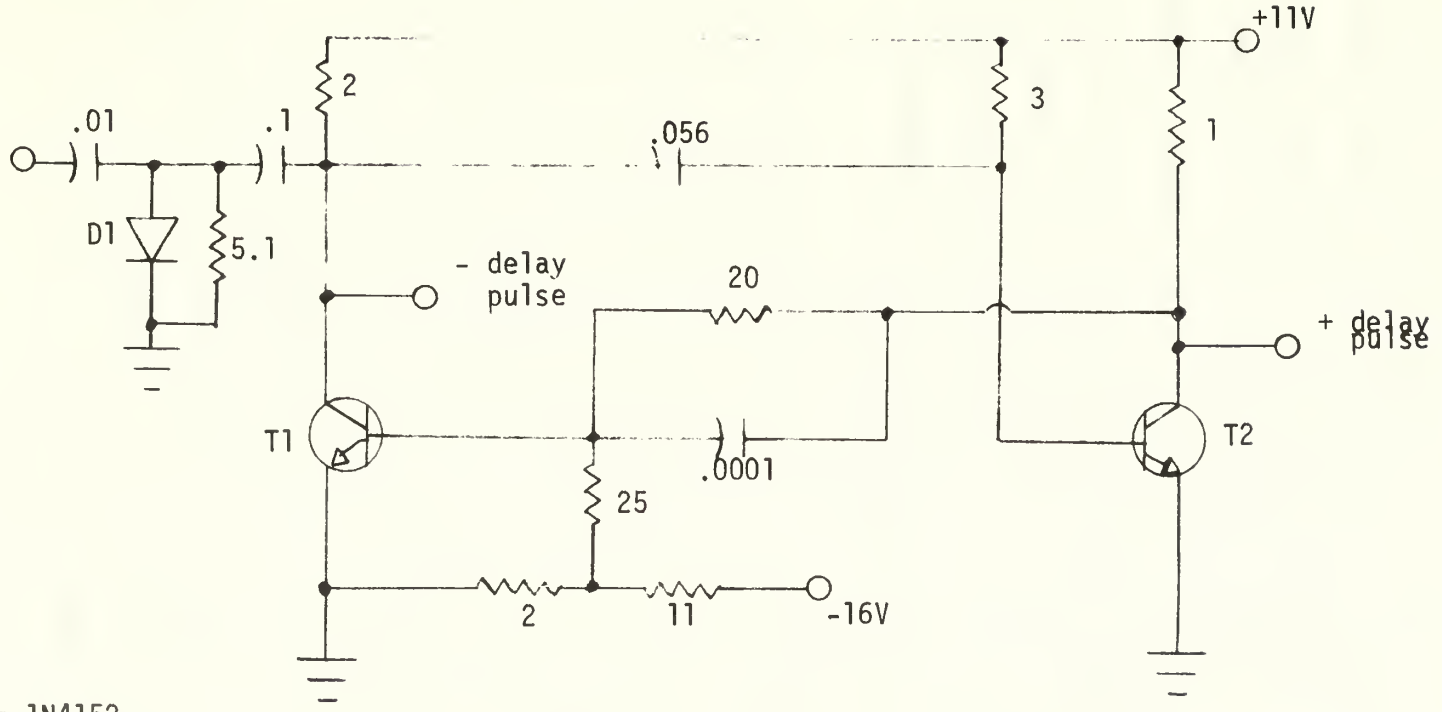
Since the diode bridge fulfills the requirements imposed upon it by the circuit, and since it also converts easily onto an integrated circuit chip, its choice is ideal for employment in the building of the proposed delay line.

III. BUILDING THE CIRCUIT

Since the expected input from the buffer amplifier in Figure 2 will vary in range from one half to one volt peak superimposed on a negative d-c value, a reasonable test input signal would be a sinusoid superimposed upon a negative d-c level. Using this test voltage, it is now possible to start building the circuit.

Before any evaluation of the delay line discussed in Chapter II is possible, it is necessary to build a monostable multivibrator to give the delayed pulses necessary for triggering the first diode switch. Many authors discuss multivibrator circuits and their application. Oppenheimer [Ref. 5] describes a monostable multivibrator which is exactly what is needed in this case. The multivibrator is triggered by a negative spike and gives positive and negative pulses at the collectors of the two transistors. The pulses are not perfectly square because by using values of capacitance and resistance such that the RC time constant forces one pulse to be square, it also causes deterioration of the other pulse. Since perfectly square pulses are not necessary, a compromise may be reached whereby both pulses are relatively square with a minimum of sag. The circuit diagram for the monostable multivibrator is shown in Figure 8.

With a pulse generator supplying positive and negative pulses and the multivibrator supplying positive and negative delayed pulses, the delay line itself may be started. Since the input to the delay line



D1= 1N4152
T1= T2= 2N337
ALL CAPACITORS IN μf
ALL RESISTORS IN KΩ

Fig. 8. Monostable multivibrator

is composed of the input signal plus a fraction of the delayed output signal, a partial summation circuit can be used as an input to the delay stage until the feedback fraction is generated.

Because the input will be between one half and one volt peak, the gain on the test signal oscillator may be set randomly within this range. This sinusoid may then be amplified to approximately two volts peak to give a workable signal to the rest of the circuit. The collector output can be applied to the top of a voltage divider with the bottom grounded and the output taken off the center tap. The required fraction of output voltage can be added to the bottom of the voltage divider once the voltage fraction has been generated. This center-tap output can now be applied to the diode-bridge sampling gate. This circuit is shown in Figure 9.

The signal applied to the diode sampling gate must have a d-c return tied to ground so that the sampled signal is passed undistorted. Switching diodes are used to obtain rapid opening of the diode bridge. The diode sampling gate itself is complete once the trigger pulses are applied to it. The circuitry of a typical diode bridge is shown in Figure 10, and is the same for all diode bridges in the system, although there are some differences in pulses applied to them.

The signal sample obtained through the diode bridge is stored on a capacitor and is then transferred through the delay bridge to a second storage capacitor. At this point it becomes necessary to incorporate isolation circuits. Within each delay line the sampling gate and the second switch are being gated on by the same trigger

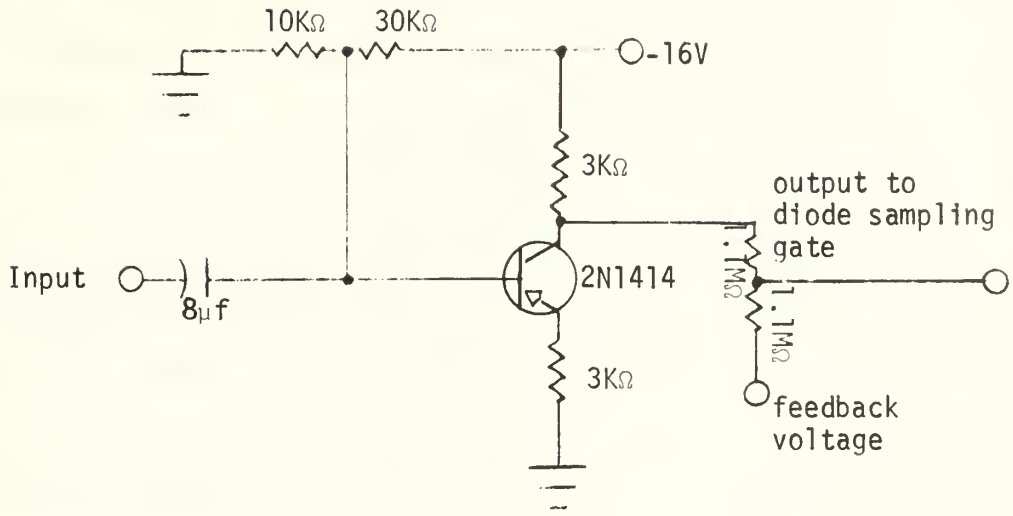


Fig. 9. Input amplifier and partial addition

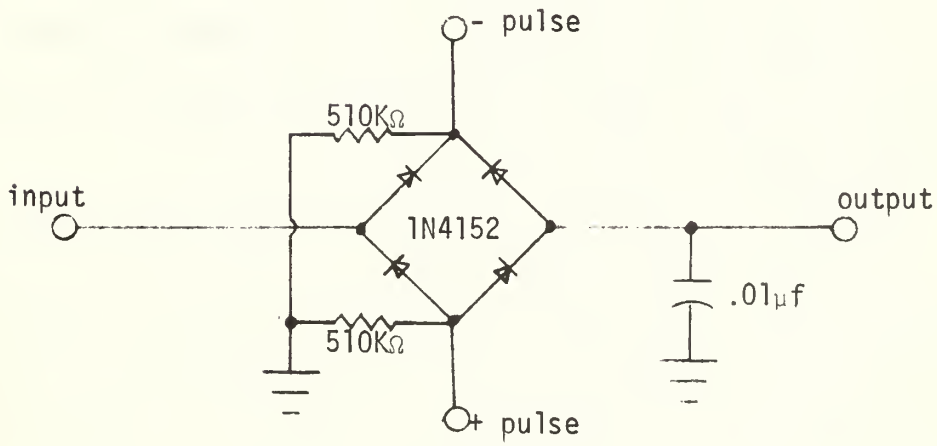


Fig. 10. Typical diode bridge

pulses. During the on time all four points in the delay bridge are connected together through low-impedance diodes. If no isolation were provided the input half of the sampling bridge would be coupled to the output half of the second diode switch, and its output would not be a delayed replica of the input, but rather the input itself.

To prevent shorting of input to output, pulse isolation circuits are incorporated between successive diode bridges using the same trigger pulses. Since the block diagram calls for three delay lines, there will be six bridges gated by trigger pulses and three bridges gated by the delayed trigger pulses. The pulses triggering each of the six undelayed diode bridges will have to be isolated from each other as will the delayed pulses triggering the three delay bridges. The isolation circuits used are the simple transistor configurations shown in Figure 11 and Figure 12.

The output of the third diode bridge is a replica of the output of the first diode bridge but delayed in time by 1.25 msec. This final output is now attenuated to give the proper feedback fraction and added to the input of the delay line by adding it to the bottom of the voltage divider in Figure 9.

This portion of the complete circuit can be tested by itself. The response should remain essentially constant throughout the frequency range with only a slight dip at mid-frequencies. By the comparison shown in Figure 13, it is seen that at frequencies in the vicinity of 400 cycles per second, the response drops below the theoretical. At low frequencies or as the frequency approaches the pulse repetition frequency there are many samples during each cycle

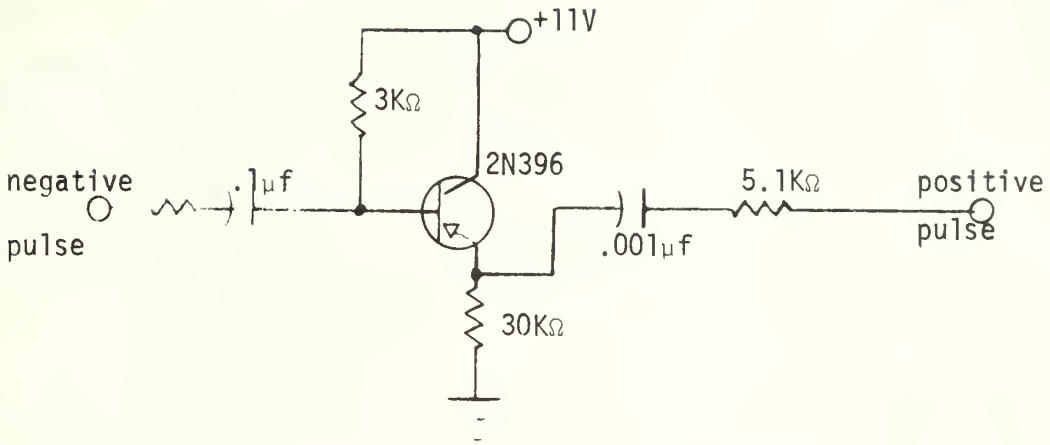


Fig. 11. Negative pulse isolation

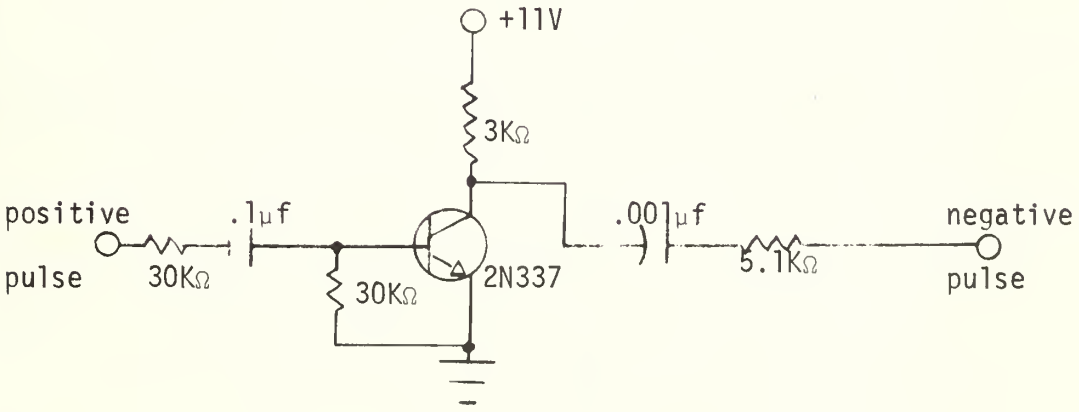


Fig. 12. Positive pulse isolation

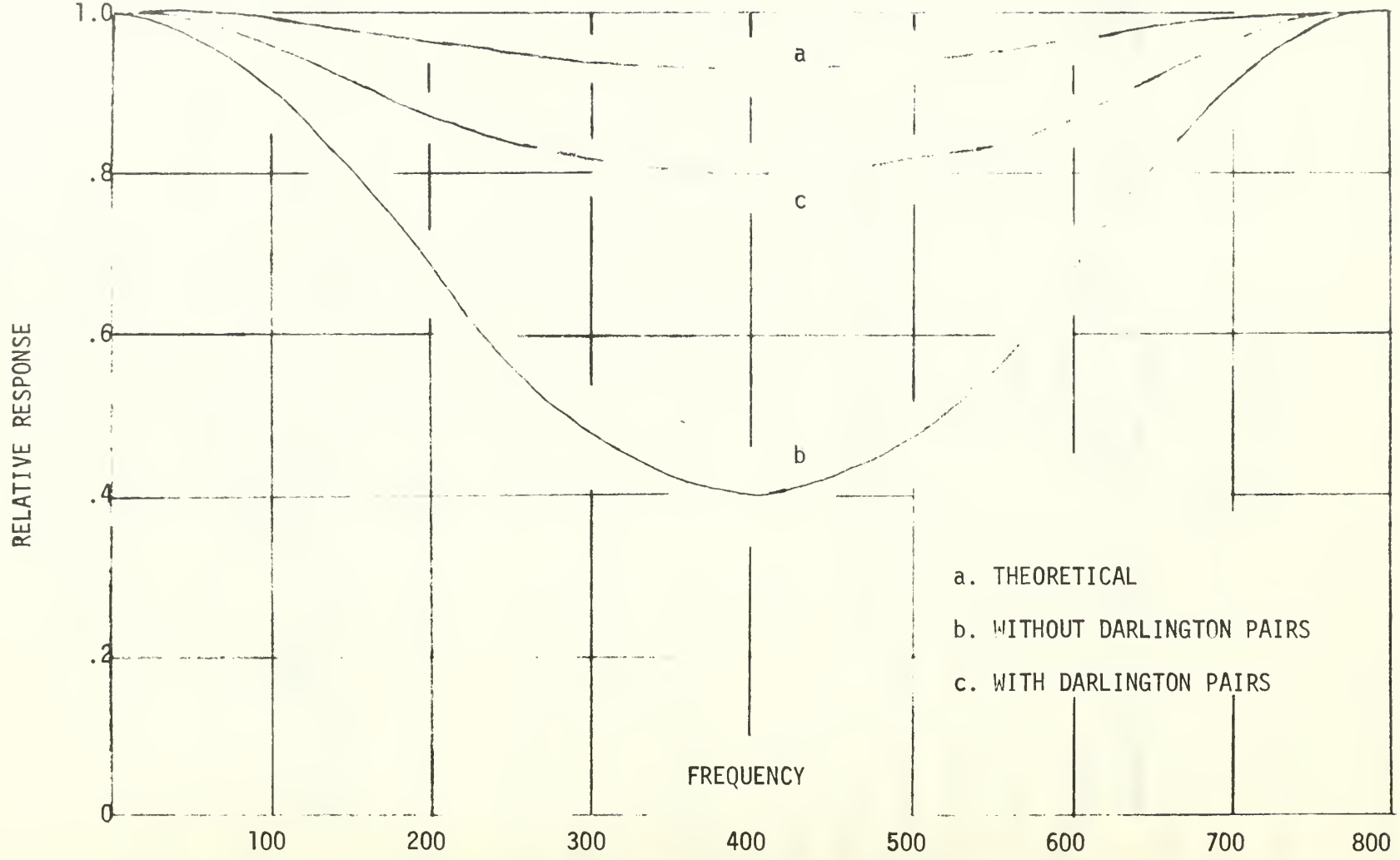


Fig. 13. Frequency comparison

of the sine wave and the capacitor is forced to accept only small changes in voltage between each sample. Near 400 cycles per second there are two samples during every cycle of the input sine wave. Therefore, at the storage capacitor, the voltage may have to change between the maximum positive excursion and the maximum negative excursion of the input sinusoid, depending upon the phase relationship. If the samples are occurring at 90^{o} and at 270^{o} on the sine function, then the maximum change takes place. If the samples occur at 0^{o} and 180^{o} on the sine function then the output is zero. Thus, the storage capacitor sometimes has to change between the positive and negative average values of the sine wave, but when sampling occurs at 0^{o} and 180^{o}, the samples are all zero no matter how large the sine wave. It is possible to force the capacitor to accept the large mid-frequency voltage excursions that may occur by increasing the current drive through the diode bridge during the on period. One method of doing this is to place Darlington pairs before each diode bridge. Thus when each bridge is gated on, the current drive through the gate and to the storage element is much greater than before. This enables the storage element to accept all voltage changes whether they are small as at low frequencies or frequencies near the pulse repetition frequency or high as will be the case near 400 cycles per second. Figure 14 shows the Darlington pair configuration which precedes each diode bridge in the circuit.

The current gain for a Darlington pair is β^{2}, and the large emitter resistors cause most of the amplified current to charge the

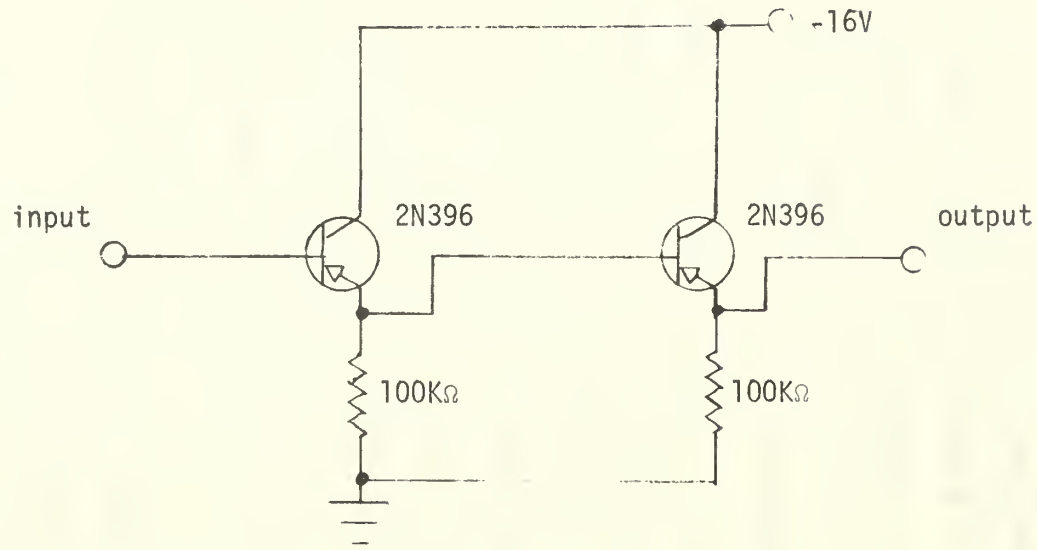


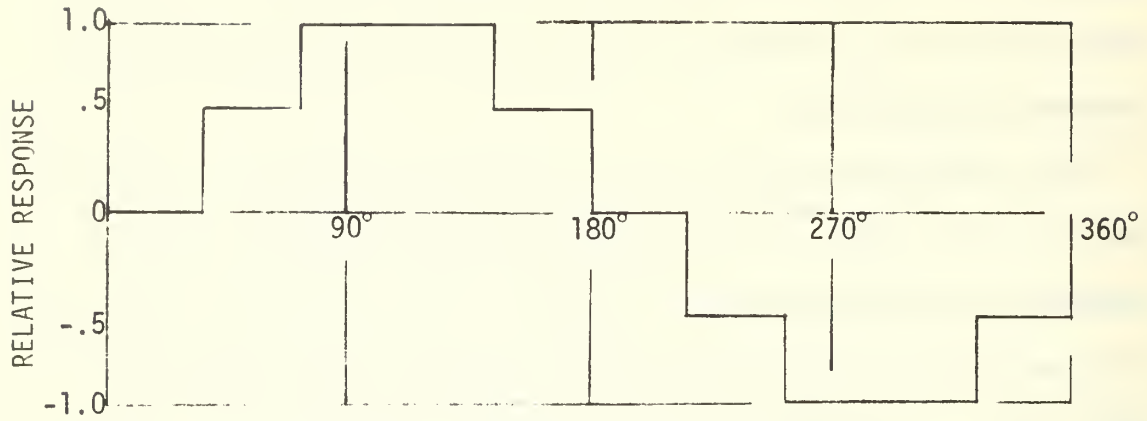
Fig. 14. Darlington pair

storage capacitor during the gated on period since only a small portion of it is bled off through the resistors to ground. With the Darlington pairs, the frequency response is much improved over that obtained without them.

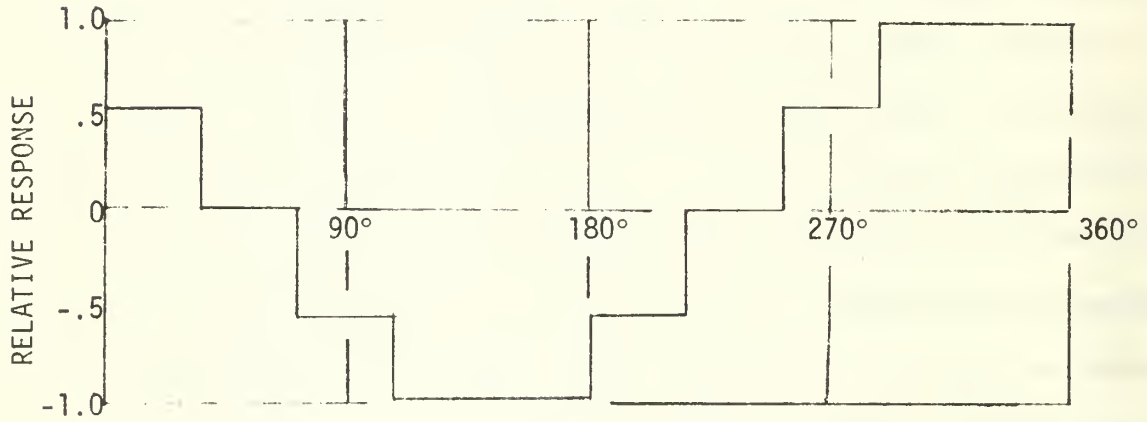
With the proper amplification to regain any voltage lost through the delay line and to invert the signal, delay cancellation may be achieved by the method shown in Figure 5. For an input sine wave at a frequency of 80 cycles per second, there will be ten samples on every cycle. The wave forms for the positive input signal, negative delayed signal and the sum of the two signals for the given conditions are shown in Figure 15. The output of the summation process is extremely small due partially to the fact that the cancellation results in a small signal and secondly that the method of addition yields only one half of the sum. This loss of amplitude necessitates the use of an additional amplifier stage to give an output large enough to drive the rest of the filter. The collector output of this amplifier stage is the value V_1 shown in Figure 3. The complete circuit diagram is shown in Figures 16a and 16b. The monostable multivibrator and all the pulse isolation circuits are omitted since they have already been shown, and would only confuse the diagram.

The second stage of the filter is simply a reproduction of the first stage with slight variations. In the first stage the feedback fraction is generated from the output of the delay line. In the second stage there are two delays, but only the final one generates the feedback voltages. It is therefore necessary to have two

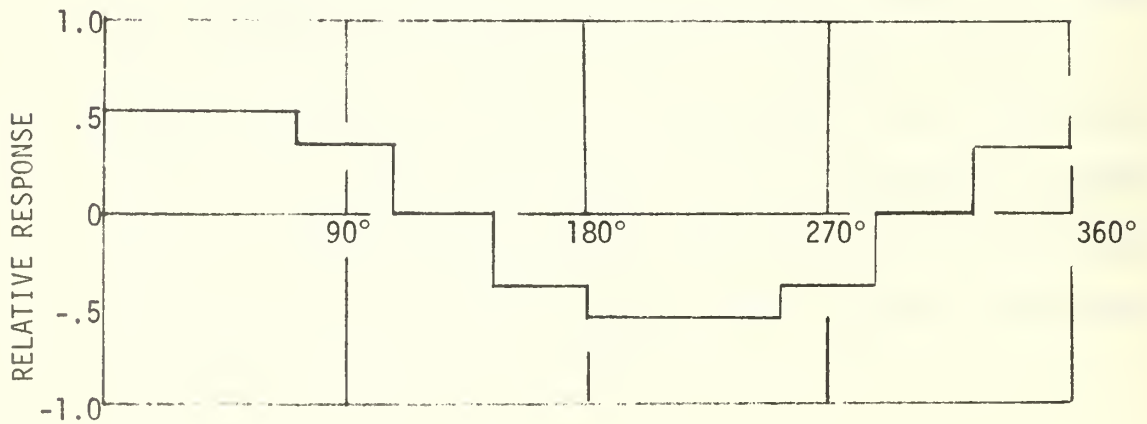
Fig. 15. Waveforms with 80 cps input signal



SAMPLED INPUT SINE WAVE



NEGATIVE DELAYED INPUT SINE WAVE



SUMMATION

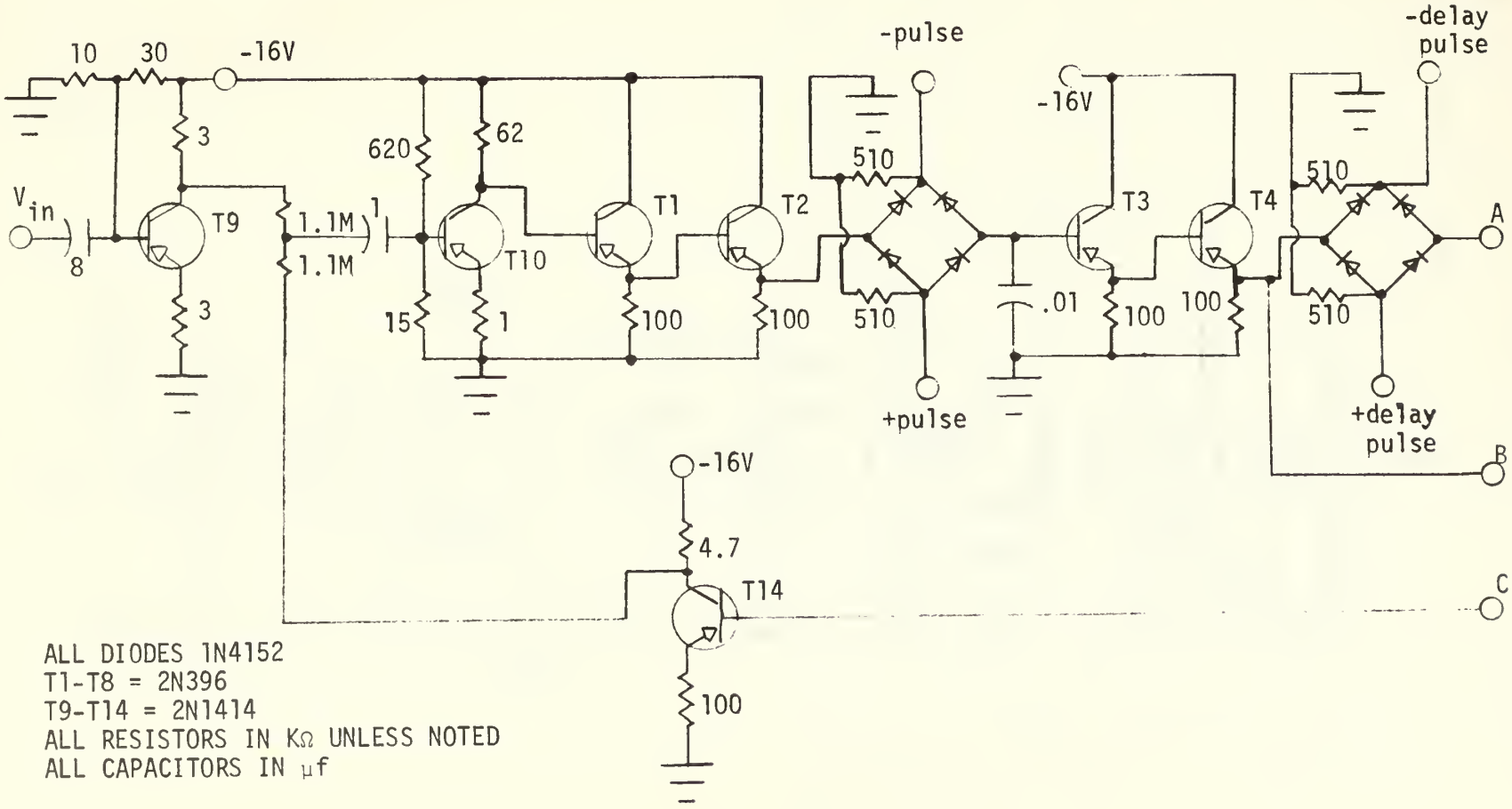


Fig. 16a. First stage

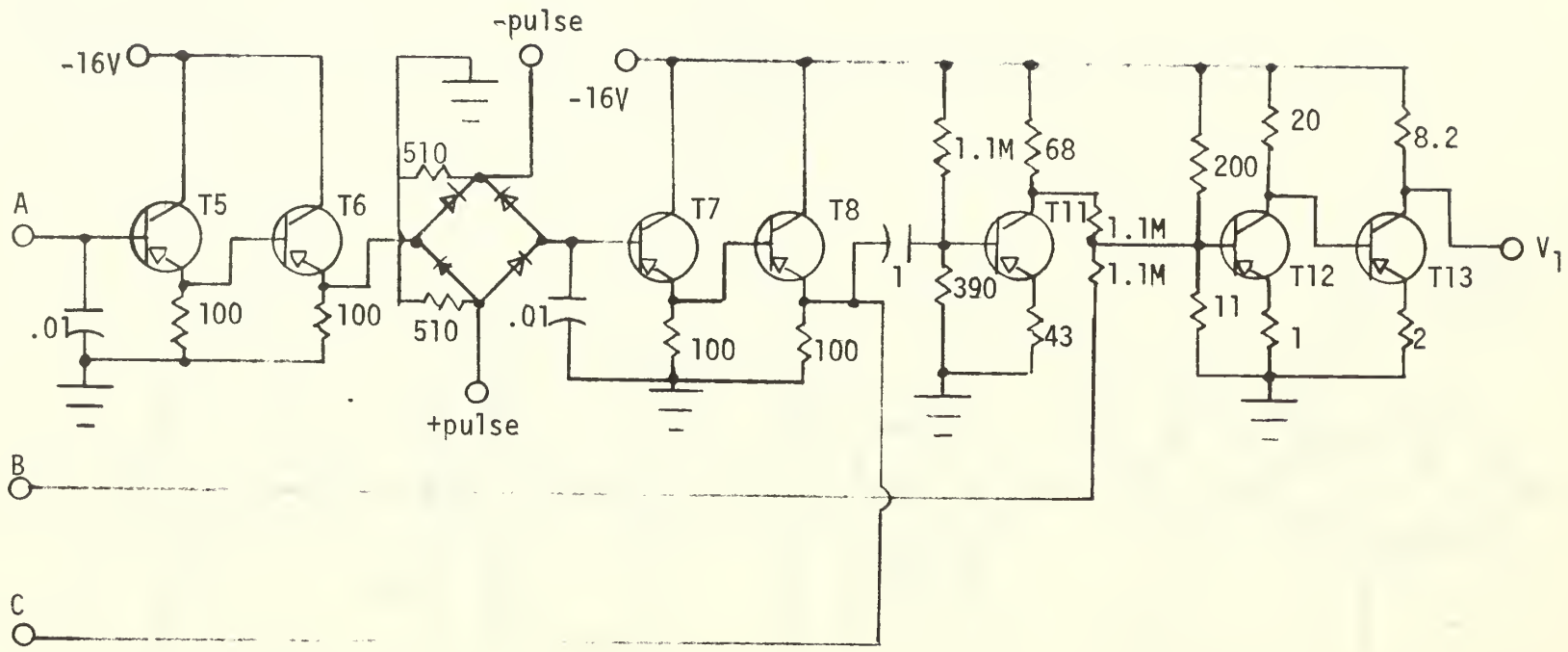

-pulse
-16V
-16V
510
A
T5
T6
T7
T8
T11
T12
T13
V_1
1.1M
68
200
20
8.2
1.1M
1.1M
.01
100
100
510
.01
100
100
1
390
43
11
1
2
+pulse
B
C

Fig. 16b.

amplifier stages each fed by the output of the final delay line in order to obtain the proper values of voltage to be added with the respective delay-line inputs.

As in stage one, the second stage requires that each trigger pulse be isolated from the preceeding one, Darlington pairs be used to increase the current drive to the storage elements, and amplifiers be used to regain voltage lost in the various addition stages. A circuit diagram for stage two is shown in Figures 17a through 17d.

Polaroid pictures of the sinusoid input to the circuit and the output at various frequencies are shown in Appendix C. The likeness between the first and second halves of the response over the frequency range of interest can be seen by comparing zero and 800 cycles per second, 100 and 700 cycles per second, 200 and 600 cycles per second, and 300 and 500 cycles per second. This response then repeats itself at intervals of 800 cycles per second.

ALL DIODES 1N4152
T1-T16 = 2N396
T17-T27 = 2N1414

ALL RESISTORS IN KΩ UNLESS NOTED
ALL CAPACITORS IN μf

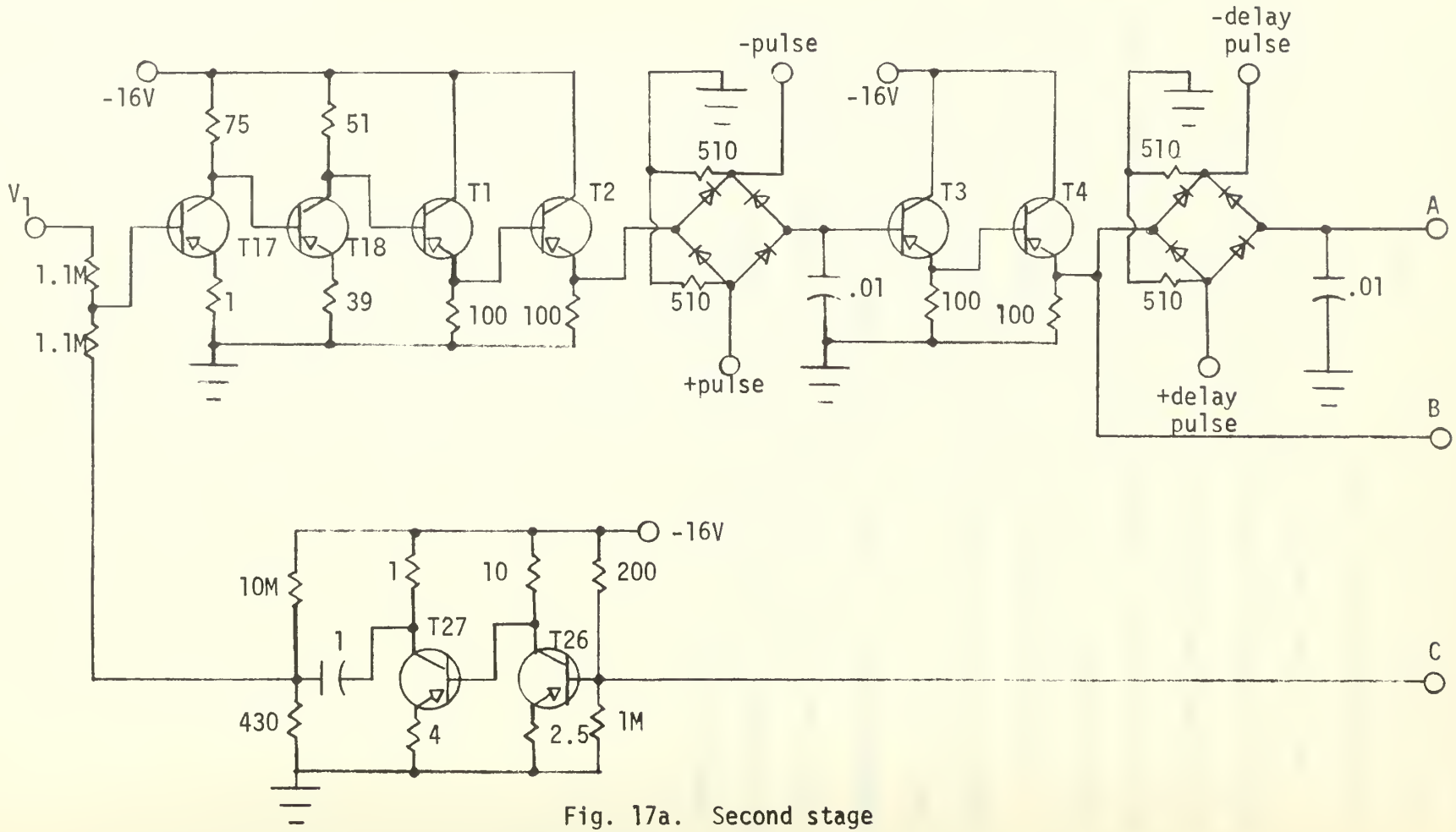


Fig. 17a. Second stage

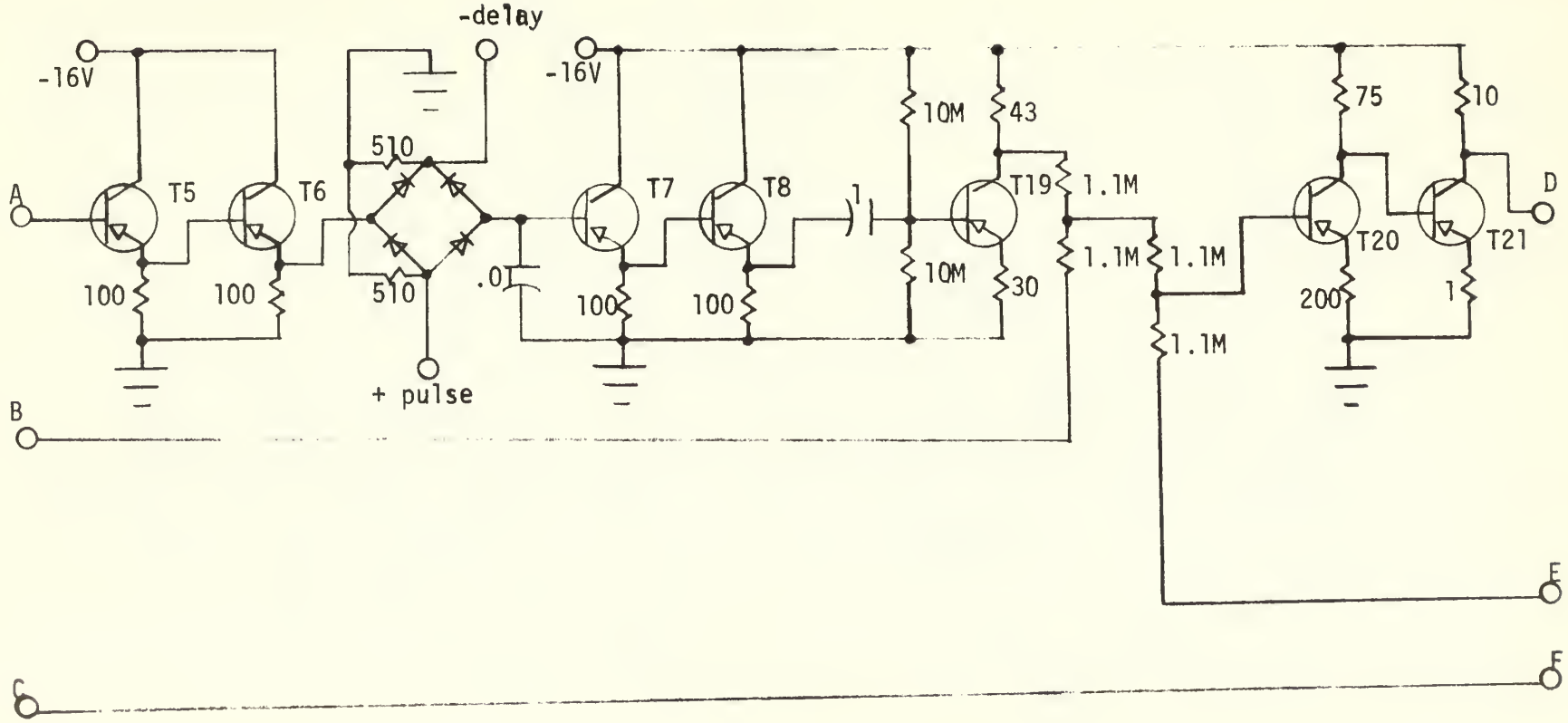

-delay
-16V
-16V
510
A
T5
T6
T7
T8
T19
T20
T21
D
100
100
510
.01
100
100
1
10M
43
10M
30
1.1M
1.1M
1.1M
1.1M
75
10
200
1
+ pulse
B
E
C
F

Fig. 17b.

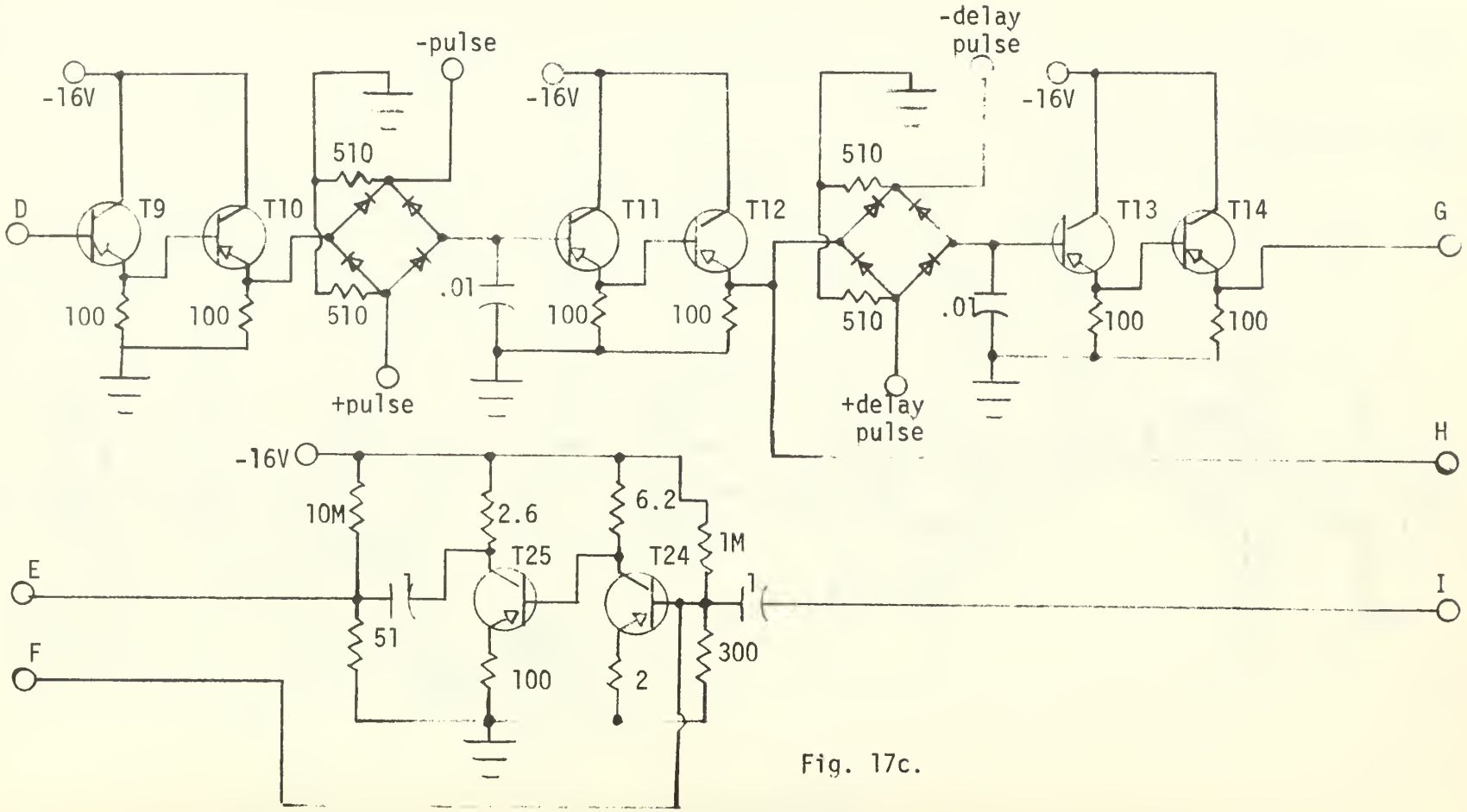

-16V
D
T9
T10
100
100
510
-pulse
+pulse
.01
T11
T12
-delay
pulse
+delay
pulse
T13
T14
G
H
I
-16V
10M
2.6
6.2
1M
T25
T24
E
F
51
100
2
300

Fig. 17c.

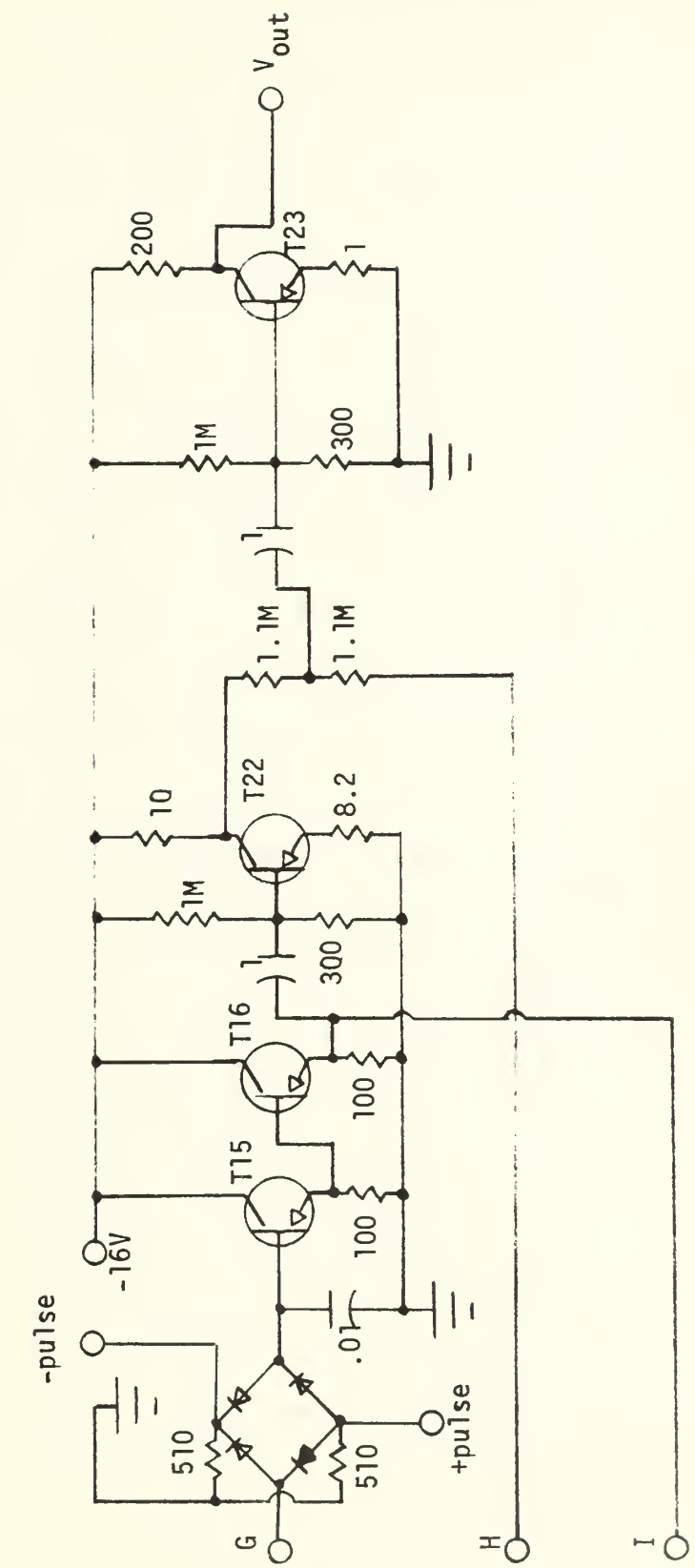

V_{out}
200
T23
1
1M
300
1.1M
1.1M
10
T22
8.2
1M
300
T16
100
T15
100
-16V
.01
-pulse
+pulse
510
510
G
H
I

Fig. 17d.

IV. COMPARISON WITH THEORETICAL

In order to evaluate the effectiveness of the filter, the design and construction of which was described in Chapters II and III, it is necessary to compare its frequency response with the theoretical responses shown in Appendix B.

Trying to read voltage values from the oscilloscope is inaccurate and not suitable for taking the required frequency response. A vacuum-tube voltmeter (VTVM) is much more reliable. By taking the ratio of output to input at various frequencies between zero and 800 cycles per second and normalizing the results, a graph of relative response versus frequency can be plotted. The experimental data for stage one, stage two and for the entire circuit is shown in Tables I, II and III respectively, and the plots corresponding to this data are shown in Figures 18, 19 and 20.

The most noticeable discrepancy between the theoretical and the designed filter is the droop at mid-frequencies. Theory shows that the relative response for the filter at 400 cycles per second should be about .99. The cancellation filter falls to slightly less than .7 at this frequency. The fault can be traced in part to the second-stage frequency response, which falls .21 below the theoretical value. This points out that the problem of the large voltage change across the storage capacitor at mid-frequencies is not completely solved by the Darlington pairs. Since the phase relationship between the input test sine wave and sampling times is not

TABLE I

Frequency Response For Cancellation Filter

First Stage

f(Hz)	Relative Response	f(Hz)	Relative Response
20	0.236	30	0.346
40	0.441	50	0.536
60	0.598	70	0.634
80	0.712	90	0.726
100	0.742	110	0.788
120	0.820	130	0.834
140	0.849	150	0.849
160	0.867	170	0.880
180	0.913	190	0.943
200	0.914	210	0.879
220	0.879	230	0.879
240	0.879	250	0.879
260	0.879	270	0.879
280	0.849	290	0.865
300	0.895	310	0.926
320	0.926	330	0.926
340	0.895	350	0.913
360	0.910	370	0.956
380	0.972	390	1.000
400	1.000	410	0.972
420	0.972	430	0.972
440	0.956	450	0.926
460	0.926	470	0.926
480	0.913	490	0.913
500	0.913	510	0.895
520	0.879	530	0.849
540	0.836	550	0.849
560	0.849	570	0.879
580	0.879	590	0.849
600	0.849	610	0.836
620	0.836	630	0.849
640	0.849	650	0.821
660	0.821	670	0.775
680	0.728	690	0.728
700	0.728	710	0.685
720	0.652	730	0.608
740	0.563	750	0.517
760	0.502	770	0.425
780	0.530	790	0.274
800	0.000		

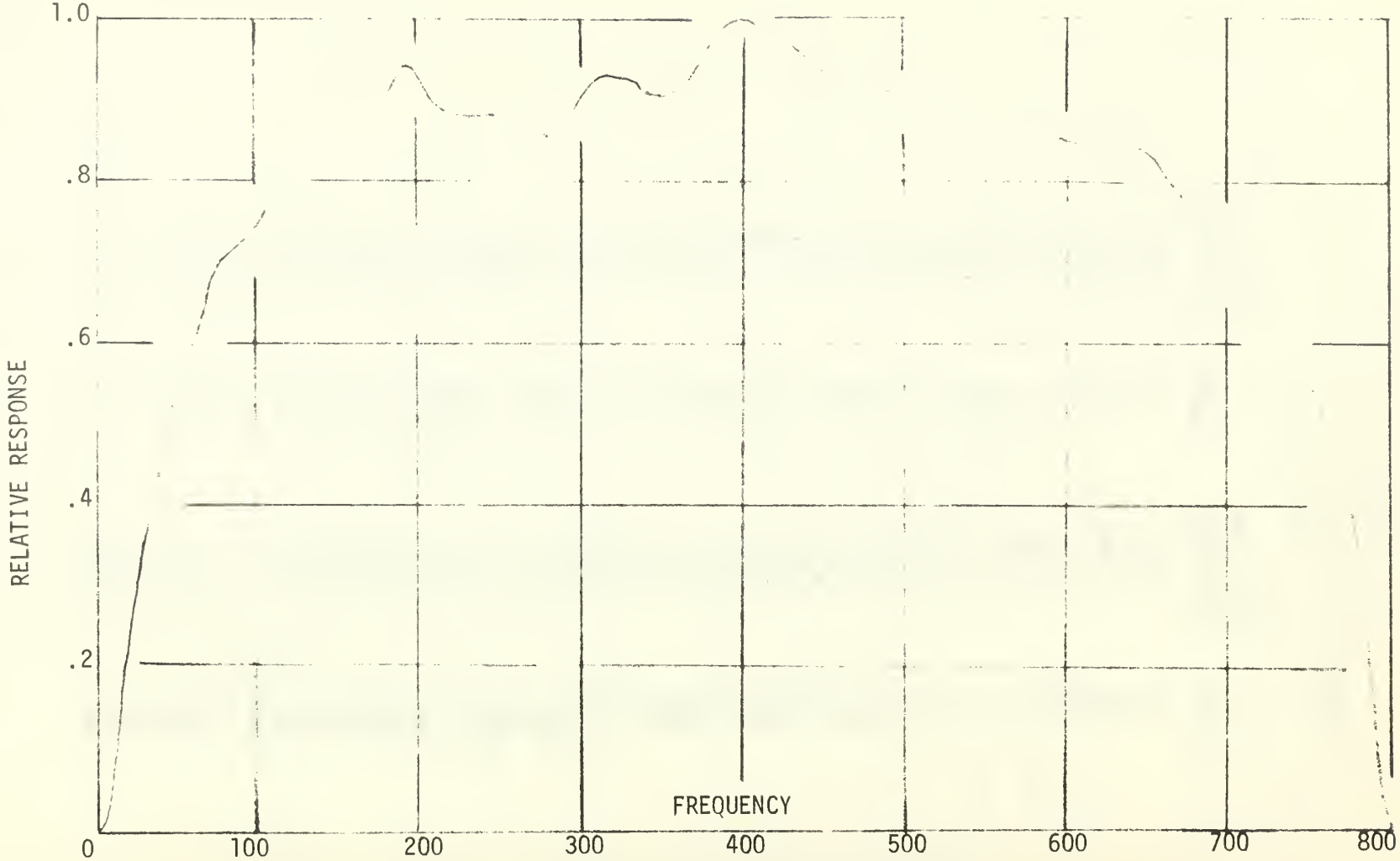


Fig. 18. First-stage response

TABLE II

Frequency Response For Cancellation Filter

Second Stage

f(Hz)	Relative Response	f(Hz)	Relative Response
20	0.075	30	0.099
40	0.181	50	0.343
60	0.532	70	0.598
80	0.728	90	0.856
100	0.934	110	0.949
120	0.974	130	0.988
140	1.000	150	1.000
160	0.961	170	0.961
180	0.921	190	0.883
200	0.856	210	0.844
220	0.823	230	0.833
240	0.817	250	0.794
260	0.728	270	0.676
280	0.676	290	0.650
300	0.676	310	0.756
320	0.804	330	0.833
340	0.856	350	0.833
360	0.779	370	0.702
380	0.598	390	0.441
400	0.334	410	0.343
420	0.330	430	0.317
440	0.364	450	0.441
460	0.546	470	0.636
480	0.689	490	0.715
500	0.756	510	0.754
520	0.728	530	0.650
540	0.636	550	0.623
560	0.634	570	0.648
580	0.687	590	0.728
600	0.756	610	0.806
620	0.834	630	0.854
640	0.898	650	0.965
660	0.989	670	0.935
680	0.898	690	0.872
700	0.834	710	0.700
720	0.634	730	0.581
740	0.541	750	0.489
760	0.409	770	0.330
780	0.158	790	0.079
800	0.000		

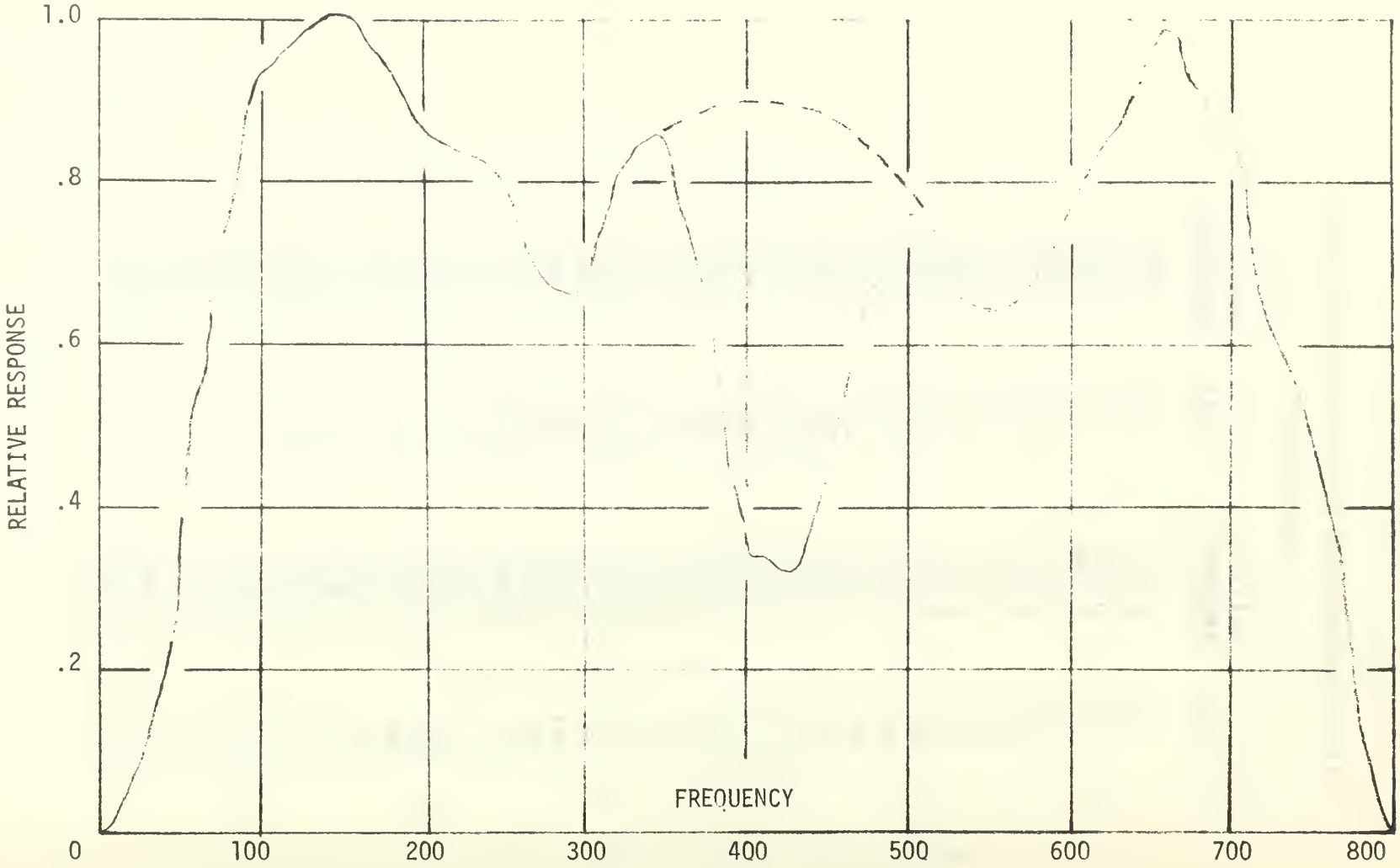


Fig. 19. Second-stage response

TABLE III

Frequency Response For Cancellation Filter

Entire Circuit

f(Hz)	Relative Response	f(Hz)	Relative Response
20	0.037	30	0.061
40	0.120	50	0.234
60	0.524	70	0.650
80	0.702	90	0.748
100	0.794	110	0.804
120	0.818	130	0.852
140	0.876	150	0.899
160	0.934	170	0.968
180	0.978	190	1.000
200	1.000	210	0.968
220	0.968	230	0.956
240	0.934	250	0.912
260	0.903	270	0.893
280	0.912	290	0.868
300	0.822	310	0.776
320	0.787	330	0.799
340	0.754	350	0.754
360	0.776	370	0.776
380	0.695	390	0.695
400	0.685	410	0.685
420	0.685	430	0.695
440	0.708	450	0.776
460	0.788	470	0.776
480	0.764	490	0.764
500	0.822	510	0.822
520	0.869	530	0.857
540	0.934	550	0.924
560	0.947	570	0.947
580	0.957	590	0.968
600	0.982	610	0.982
620	0.957	630	0.947
640	0.926	650	0.912
660	0.888	670	0.864
680	0.844	690	0.822
700	0.799	710	0.776
720	0.731	730	0.683
740	0.641	750	0.524
760	0.251	770	0.136
780	0.068	790	0.023
800	0.000		

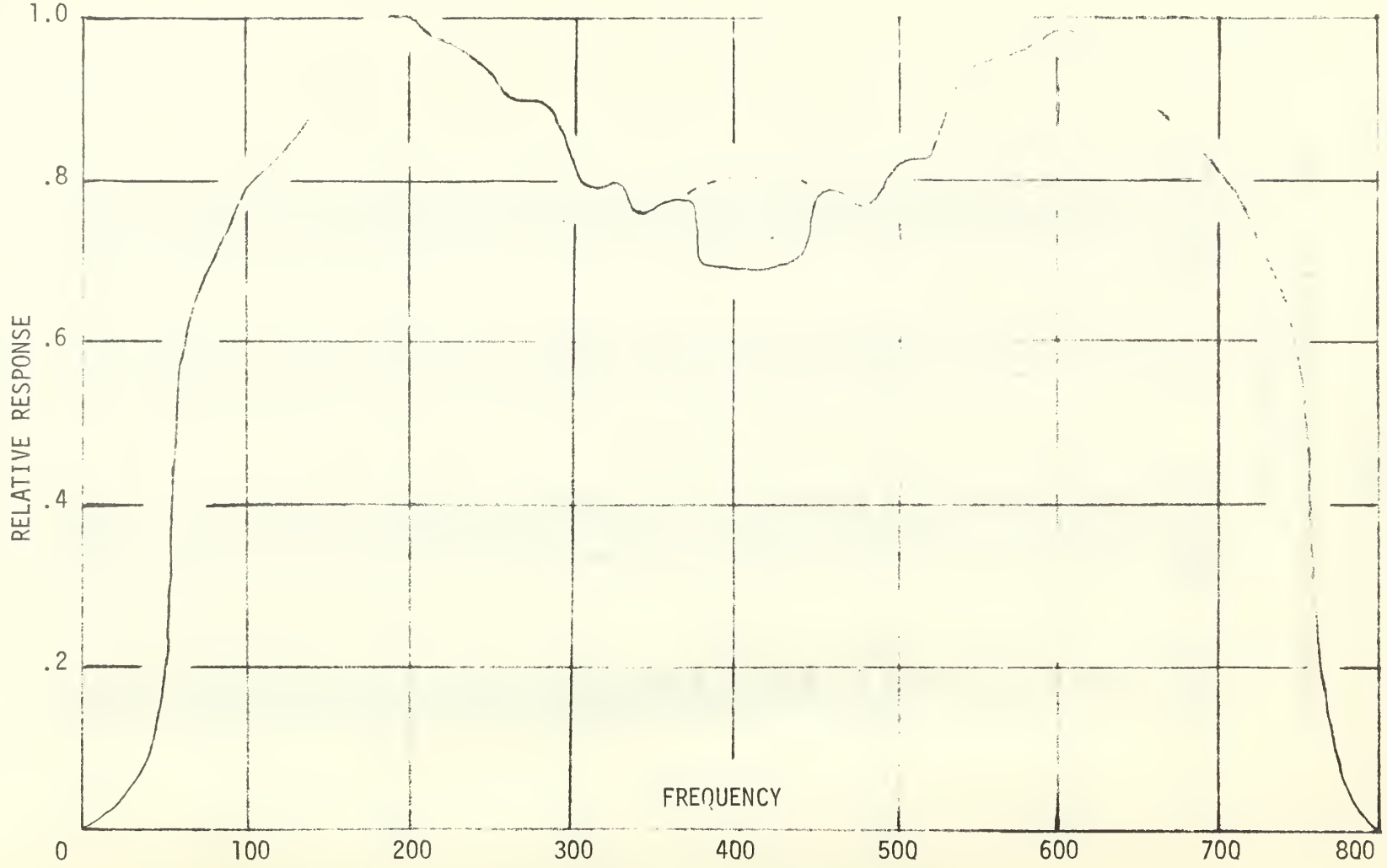


Fig. 20. Entire circuit response

always optimum near 400 cycles, the output would be expected to fall off somewhat. For this reason, the values recorded in the vicinity of 400 cycles per second fall off. By referring to Figure 19 and Figure 20 it is seen that for frequencies between 340 cycles per second and 510 cycles per second on the second-stage response, and for frequencies betwen 380 cycles per second and 440 cycles per second on the final response, the data changes radically from the established trends indicated by dashed lines on the respective responses.

The peaks of the passband for the cancellation filter occur 40 cycles per second closer to mid-frequency than calculations would indicate. This shift is not overly harmful since the filter response retains high passband characteristics over approximately the same range as the theoretical model.

Half-power points are another area for comparison. The model has half-power points at 105 cycles per second and 695 cycles per second, while in the cancellation filter they occur at 60 cycles per second and 750 cycles per second. The wider passband, however, does not destroy the rejection bands at zero and multiples of the pulse repetition frequency. Although not quite as good as the calculated values, the amount of clutter rejection given by the filter is still substantial.

Since the filter was built on vector board and never reduced to a prototype, some of the discrepancies between the theoretical and actual frequency responses may be due to poor connections associated with unsoldered joints and to the stray capacitances associated with the long wires.

A greater part of the discrepancy is probably due to inaccuracy in the voltages being added in the summing circuits, especially those circuits that perform the cancellation. In these circuits the delayed voltage must be an exact negative replica of the undelayed voltage in order for exact cancellation to take place as in Figure 15. If this is not the case, then the output voltage will be distorted and will have a significant effect on the performance of the rest of the circuit.

Whether these voltages are exact negative replicas of one another depends largely on the storage capacitors in the delay line. These storage elements are not high-precision capacitors and are marked as being accurate to only ±10% of their rated value. Thus although the discharging time constant may calculate to be exactly the same for all the storage elements in the delay line, they may be quite different and give more voltage droop due to discharge on some capacitors than on others. The amount of droop associated with each storage element is critical in establishing exact cancellation at the output of the delay line.

The problem of droop on the storage capacitor may be solved in any future attempts at bettering this circuit design by substituting metal-oxide-semiconductor field effect transistors (MOSFET) for the diode bridges. Although the diode bridges have low on impedance, the MOSFET has even lower on impedance and is therefore better suited for this application.

In addition to simplifying the circuit and reducing the area required for integrated circuit conversion, the MOSFETs will allow

a smaller storage capacitor to be used without permitting any droop in the voltage sample to take place. The smaller capacitor coupled with the Darlington pairs will further improve the frequency response near 400 cycles per second. For further information and explanation of MOSFETs see the paper by Burd and Sear [Ref. 6].

Since this filter was designed to be used in conjunction with the range channel built by E. L. Washam, a final evaluation of it may be made by actually inserting it into Washam's range channel. With a sinusoid test voltage as the input to the entire range channel, the system functions as would be expected. Any input frequency which lies within the passband of the cancellation filter appears at the output of the range channel as a voltage pulse indicating the presence of a target within the range of this channel. Frequencies near zero or near multiples of the pulse repetition frequency corresponding to fixed target clutter are rejected by the filter, and no output appears.

Time limitations prevented incorporation of the combined range channel into a transmitting MTI radar, but since the system responded as expected to the input test sine wave, it should also perform as required in the radar.

V. CONCLUSION

This thesis was motivated by the possibility of building a cancellation filter which could be fabricated on integrated circuit chips and which would be suitable for use in a range channel of an MTI radar. It has been shown that this filter provides the relatively flat passband which is desired and the necessary rejection at zero frequency and at integer multiples of the pulse repetition frequency.

The use of enough range channels to cover the entire distance corresponding to the maximum range for MTI operation is necessary to complete the range-gated filter. The maximum range for most radars and in particular MTI type radars is less than the range corresponding to the reciprocal of the pulse repetition frequency. Each one of these range channels requires a cancellation filter with the above characteristics. If, for example, each range channel covered 2 μsec, then 480 cancellation filters would be necessary to cover a maximum range of 80 nautical miles. Beyond this range fixed clutter is seldom a problem, and normal video could be used.

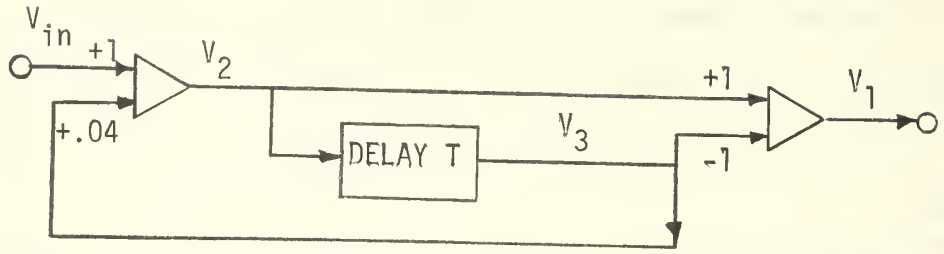
Since the above filter was designed with integrated circuitry in mind, the amount of space required by this number of integrated circuit chips would still be many times less than that taken by the three quartz delay lines required to obtain the same frequency response. The cost of the integrated circuit chips should be much less than the quartz delay lines with the added benefits of reduced weight and improved reliability.

The quartz delay line by itself is highly reliable, but since there is a large amount of attenuation associated with it, much amplification is necessary. These amplifier stages are subject to failure, and a breakdown anywhere in the system renders it inoperable. On the other hand, if one range channel breaks down the rest of the system is still functional, sacrificing less than one percent of its efficiency.

It has been demonstrated that circuits of a type that could be manufactured in integrated circuit form can be used to perform the functions of the quartz delay lines. But before such integrated circuits are made, it would be beneficial to do further research and development on the above circuit design, especially with respect to the possibility of including MOSFETs in the gating circuits.

APPENDIX A

DERIVATION OF TRANSFER FUNCTIONS



$$V_3 = (V_{in} + .04V_3)e^{-j\omega T}$$

$$V_3 = V_{in}e^{-j\omega T} + .04V_3e^{-j\omega T}$$

$$V_3(1 - .04e^{-j\omega T}) = V_{in}e^{-j\omega T}$$

$$\frac{V_3}{V_{in}} = \frac{e^{-j\omega T}}{1 - .04e^{-j\omega T}}$$

$$V_1 = (V_{in} + .04V_3)(1 - e^{-j\omega T})$$

$$V_1 = V_{in}(1 + .04\,\frac{V_3}{V_{in}})(1 - e^{-j\omega T})$$

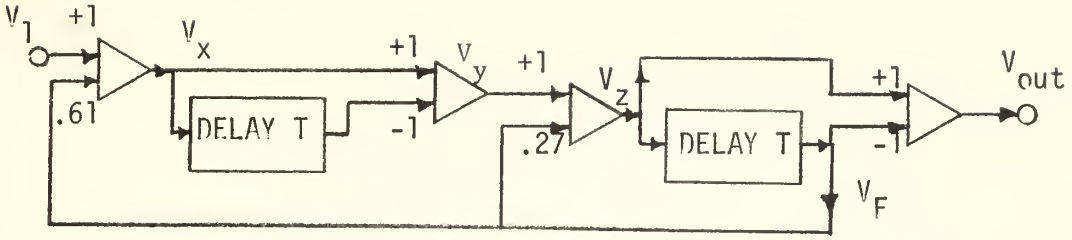
$$V_1 = V_{in}[1 + .04(\frac{e^{-j\omega T}}{1 - .04e^{-j\omega T}})]\ (1 - e^{-j\omega T})$$

$$V_1 = V_{in}(1 + \frac{.04e^{-j\omega T}}{1 - .04e^{-j\omega T}})\ (1 - e^{-j\omega T})$$

$$\frac{V_1}{V_{in}} = \frac{1 - .04e^{-j\omega T} + .04e^{-j\omega T}}{1 - .04e^{-j\omega T}}\ (1 - e^{-j\omega T})$$

$$\frac{V_1}{V_{in}} = \frac{1 - e^{-j\omega T}}{1 - .04e^{-j\omega T}} = \frac{e^{j\omega T} - 1}{e^{j\omega T} - .04}$$

$z = e^{j\omega T}$ $\qquad H_1(z) = \dfrac{V_1}{V_{in}} = \dfrac{z - 1}{z - .04}$



$$V_y = (V_1 + .61V_F)(1 - e^{-j\omega T})$$

$$V_z = (V_1 + .61V_F)(1 - e^{-j\omega T}) + .27V_F$$

$$V_F = [(V_1 + .61V_F)(1 - e^{-j\omega T}) + .27V_F]\, e^{-j\omega T}$$

$$V_F = [.61(1 - e^{-j\omega T}) + .27]\, e^{-j\omega T} V_F + V_1(1 - e^{-j\omega T})\, e^{-j\omega T}$$

$$\frac{V_F}{V_1} = \frac{(1 - e^{-j\omega T})\, e^{-j\omega T}}{1 - [.61(1 - e^{-j\omega T}) + .27]\, e^{-j\omega T}} = \beta(1 - e^{-j\omega T})$$

$$V_{out} = V_1\left[\left(1 + .61\,\frac{V_F}{V_1}\right)(1 - e^{-j\omega T}) + .27\,\frac{V_F}{V_1}\right](1 - e^{-j\omega T})$$

$$\frac{V_{out}}{V_1} = [1 + .61\beta(1 - e^{-j\omega T}) + .27\beta](1 - e^{-j\omega T})^2$$

$$\frac{V_{out}}{V_1} = (1 + .88\beta - .61\beta e^{-j\omega T})(1 - e^{-j\omega T})^2$$

$$\beta = \frac{e^{-j\omega T}}{1 - [.61(1 - e^{-j\omega T}) + .27]\, e^{-j\omega T}}$$

$$\beta = \frac{1}{e^{j\omega T} - .88 + .61e^{-j\omega T}}$$

$$\frac{V_{out}}{V_1} = \left[1 + \frac{(.88 - .61e^{-j\omega T})}{e^{j\omega T} - .88 + .61e^{-j\omega T}}\right](1 - e^{-j\omega T})^2$$

$$\frac{V_{out}}{V_1} = \frac{e^{j\omega T} - .88 + .61e^{-j\omega T} + .88 - .61e^{-j\omega T}}{e^{j\omega T} - .88 + .61e^{-j\omega T}}\,(1 - e^{-j\omega T})^2$$

$$\frac{V_{out}}{V_1} = \frac{e^{j\omega T}}{e^{j\omega T} - .88 + .61e^{-j\omega T}} \left(1 - e^{-j\omega T}\right)^2$$

$$\frac{V_{out}}{V_1} = \frac{\left(1 - e^{-j\omega T}\right)^2}{1 - .88e^{-j\omega T} + .61e^{-j2\omega T}}$$

$$\frac{V_{out}}{V_1} = \frac{\left(e^{j\omega T} - 1\right)^2}{\left(e^{j\omega T}\right)^2 - .88e^{j\omega T} + .61}$$

$$z = e^{j\omega T}$$

$$H_2(z) = \frac{V_{out}}{V_1} = \frac{(z - 1)^2}{z^2 - .88z + .61}$$

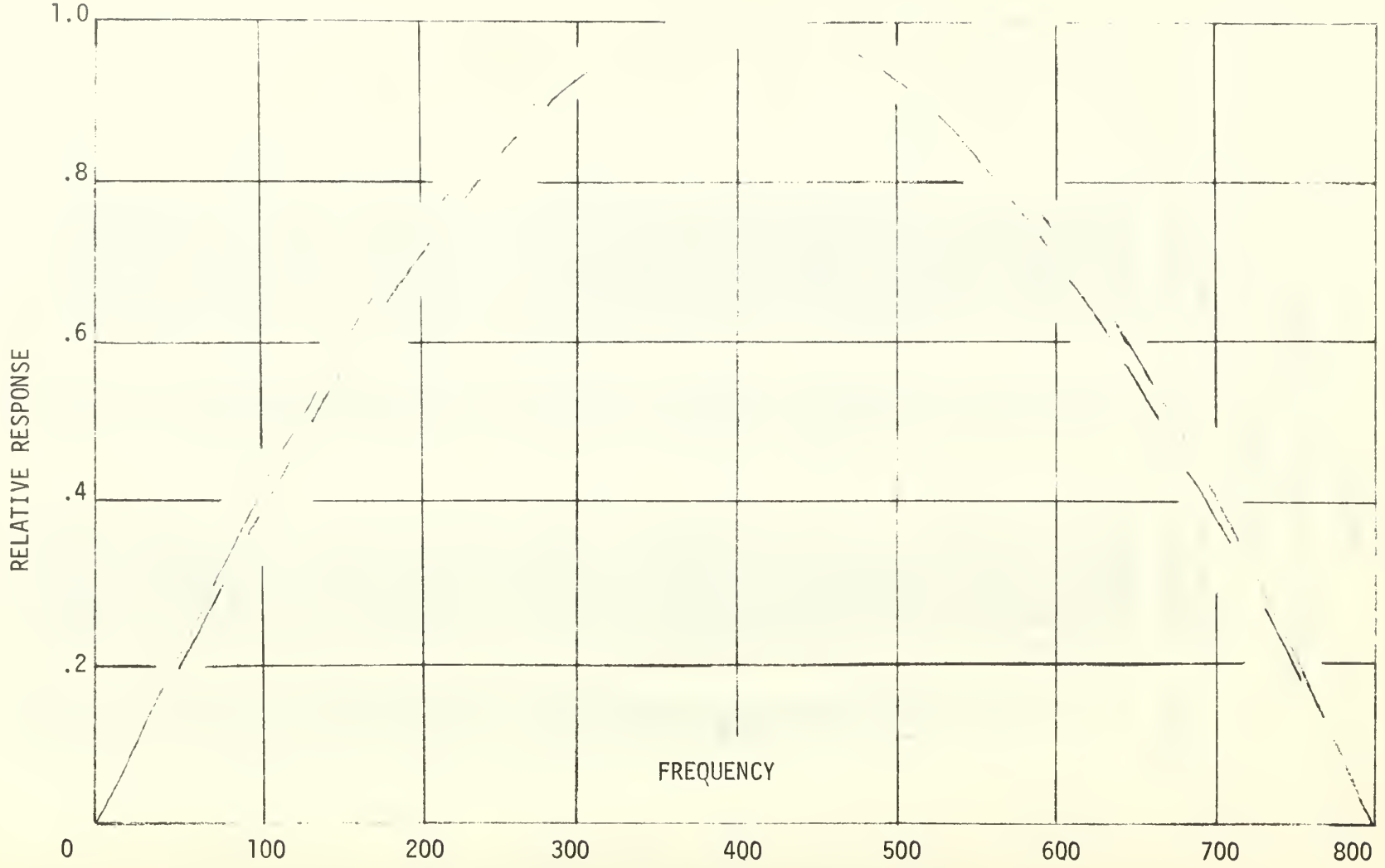
$$H(z) = H_1(z)\, H_2(z) = \frac{(z - 1)^3}{(z - .04)\,(z^2 - .88z + .61)}$$

APPENDIX B

Theoretical Frequency Response

First Stage

f(Hz)	Relative Response	f(Hz)	Relative Response
0	0.0000000	10	0.0425256
20	0.0849518	30	0.1271795
40	0.1691114	50	0.2106526
60	0.2517107	70	0.2921970
80	0.3320270	90	0.3711200
100	0.4094014	110	0.4468004
120	0.4832523	130	0.5186981
140	0.5530837	150	0.5863612
160	0.6184873	170	0.6494247
180	0.6791411	190	0.7076078
200	0.7348021	210	0.7607039
220	0.7852981	230	0.8085717
240	0.8305172	250	0.8511263
260	0.8703953	270	0.8883229
280	0.9049072	290	0.9201485
300	0.9340509	310	0.9466147
320	0.9578441	330	0.9677420
340	0.9763118	350	0.9835566
360	0.9894792	370	0.9940842
380	0.9973711	390	0.9993419
400	1.0000000	410	0.9993424
420	0.9973722	430	0.9940842
440	0.9894792	450	0.9835570
460	0.9763123	470	0.9677420
480	0.9578441	490	0.9466152
500	0.9340513	510	0.9201490
520	0.9049077	530	0.8883225
540	0.8703963	550	0.8511267
560	0.8305172	570	0.8085732
580	0.7852991	590	0.7607049
600	0.7348036	610	0.7076088
620	0.6791421	630	0.6494262
640	0.6184883	650	0.5863618
660	0.5530862	670	0.5187008
680	0.4832551	690	0.4468027
700	0.4094037	710	0.3711225
720	0.3320293	730	0.2921995
740	0.2517126	750	0.2106544
760	0.1691132	770	0.1271814
780	0.0849536	790	0.0425269
800	0.0000012		

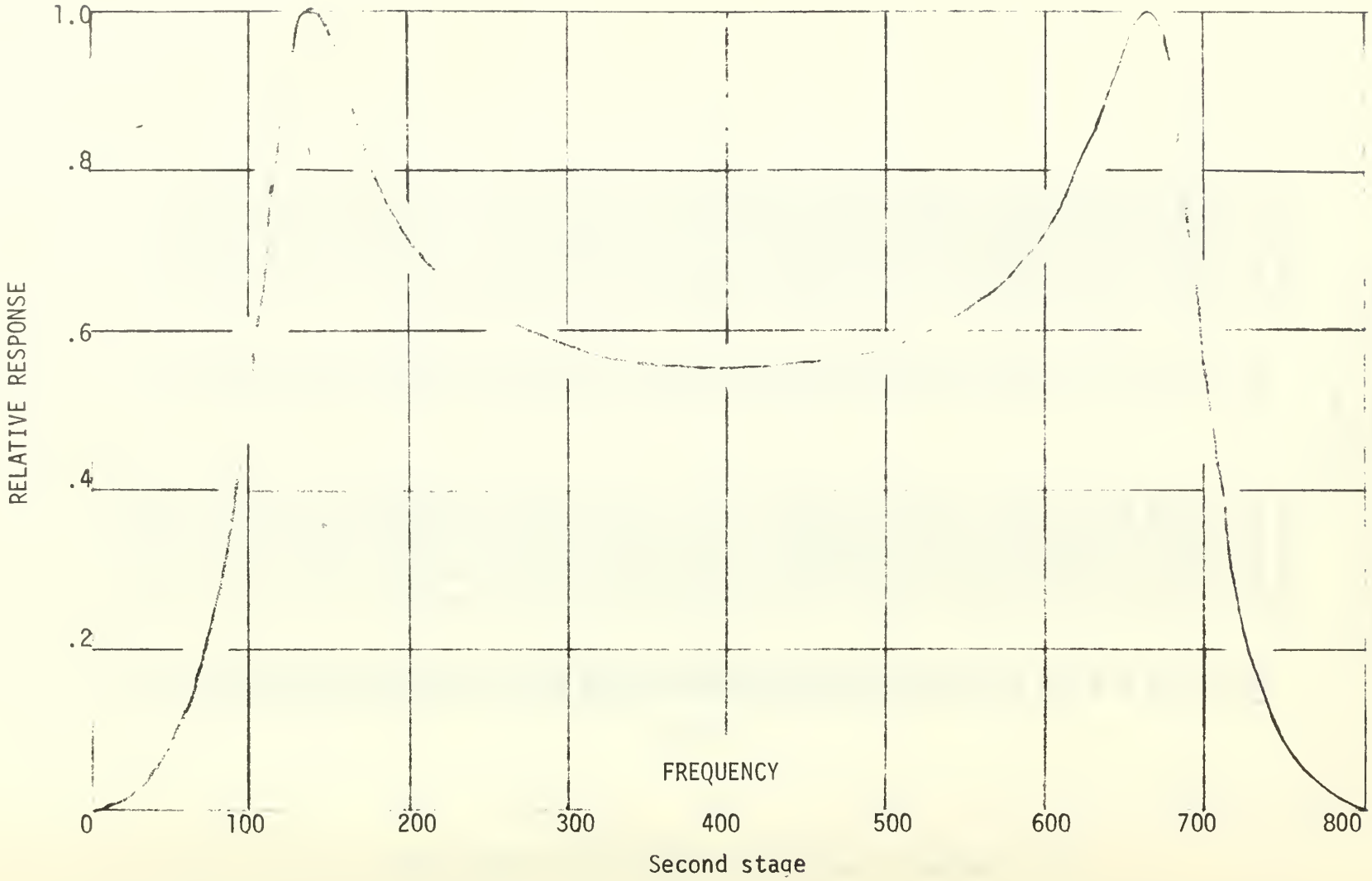


First stage (solid line) and sine wave (dashed line)

Theoretical Frequency Response

Second Stage

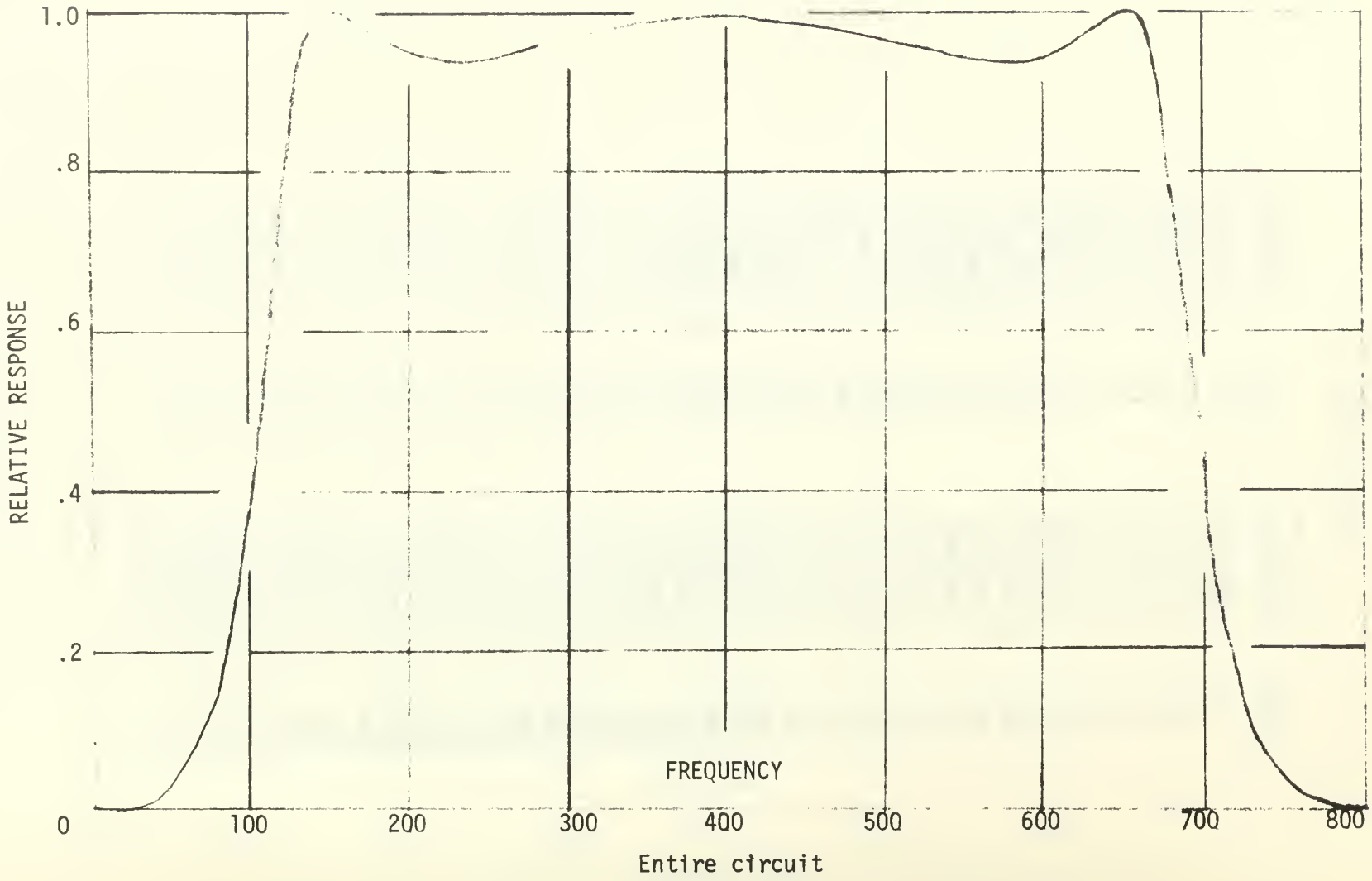
f(Hz)	Relative Response	f(Hz)	Relative Response
0	0.0000000	10	0.0029414
20	0.0119607	30	0.0276686
40	0.0511789	50	0.0842739
60	0.1296670	70	0.1913801
80	0.2751374	90	0.3882190
100	0.5366718	110	0.7147053
120	0.8853958	130	0.9877344
140	1.0000000	150	0.9572210
160	0.8981277	170	0.8414753
180	0.7928165	190	0.7525221
200	0.7194594	210	0.6922872
220	0.6698248	230	0.6511243
240	0.6354460	250	0.6222181
260	0.6109980	270	0.6014395
280	0.5932732	290	0.5862855
300	0.5803069	310	0.5752021
320	0.5708631	330	0.5672023
340	0.5641497	350	0.5616500
360	0.5596595	370	0.5581445
380	0.5570791	390	0.5564468
400	0.5562374	410	0.5564468
420	0.5570795	430	0.5581441
440	0.5596595	450	0.5616500
460	0.5641497	470	0.5672016
480	0.5708631	490	0.5752021
500	0.5803069	510	0.5862852
520	0.5932726	530	0.6014392
540	0.6109970	550	0.6222178
560	0.6354456	570	0.6511230
580	0.6698238	590	0.6922868
600	0.7194588	610	0.7525214
620	0.7928132	630	0.8414713
640	0.8981237	650	0.9572154
660	0.9999996	670	0.9877393
680	0.8854070	690	0.7147165
700	0.5366823	710	0.3882269
720	0.2751434	730	0.1913839
740	0.1296697	750	0.0842754
760	0.0511802	770	0.0276697
780	0.0119612	790	0.0029414
800	0.0000000		


1.0
.8
.6
.4
.2
RELATIVE RESPONSE
0
100
200
300
400
500
600
700
800
FREQUENCY
Second stage

Theoretical Frequency Response

Entire Circuit

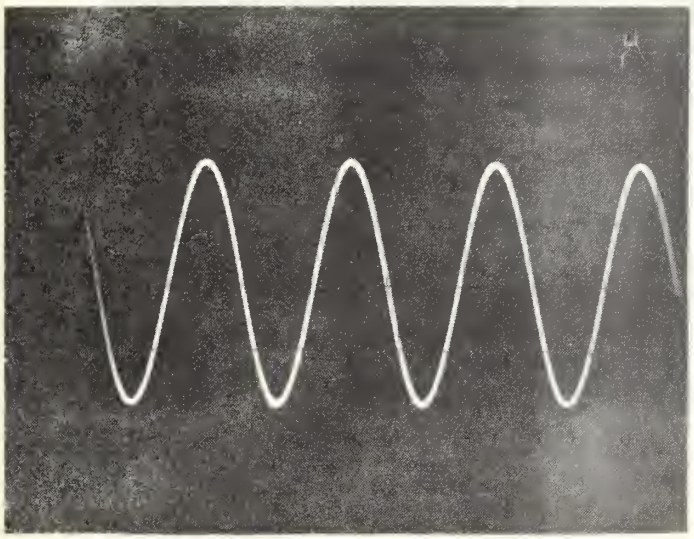
f(Hz)	Relative Response	f(Hz)	Relative Response
0	0.0000000	10	0.0002229
20	0.0018103	30	0.0062694
40	0.0154201	50	0.0316288
60	0.0581505	70	0.0996311
80	0.1627592	90	0.2566928
100	0.3914536	110	0.5689355
120	0.7623140	130	0.9128035
140	0.9854018	150	1.0000000
160	0.9896723	170	0.9736271
180	0.9593018	190	0.9487120
200	0.9418879	210	0.9382629
220	0.9371698	230	0.9380047
240	0.9402640	250	0.9435375
260	0.9474993	270	0.9518870
280	0.9564918	290	0.9611466
300	0.9657190	310	0.9700994
320	0.9742026	330	0.9779578
340	0.9813085	350	0.9842096
360	0.9866270	370	0.9885355
380	0.9099113	390	0.9907413
400	0.9910206	410	0.9907418
420	0.9899127	430	0.9885349
440	0.9866270	450	0.9842102
460	0.9813088	470	0.9779567
480	0.9742026	490	0.9701000
500	0.9657196	510	0.9611466
520	0.0564915	530	0.9518860
540	0.9474987	550	0.9435375
560	0.9402633	570	0.9380044
580	0.9371698	590	0.9382635
600	0.9418887	610	0.9487126
620	0.9592991	630	0.9736246
640	0.9896696	650	0.9999951
660	0.9854058	670	0.9128130
680	0.7623280	690	0.5689474
700	0.3914637	710	0.2566998
720	0.1627639	730	0.0996339
740	0.0581522	750	0.0316296
760	0.0154206	770	0.0062697
780	0.0018104	790	0.0002229
800	0.0000000		



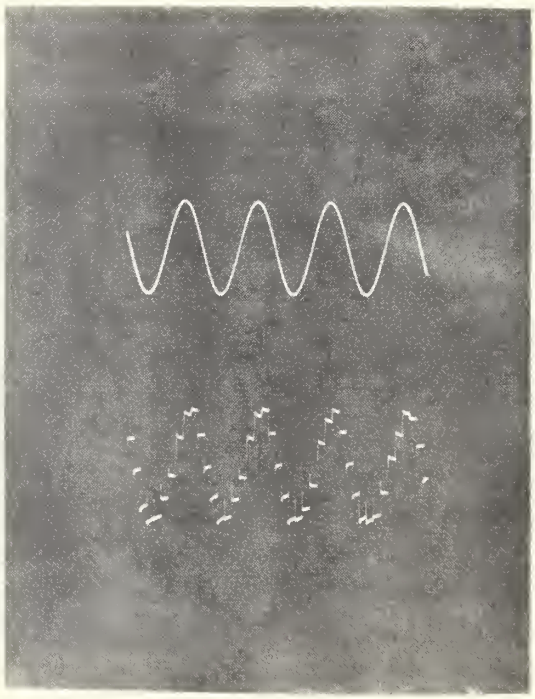
Entire circuit

APPENDIX C

PHOTOGRAPHS

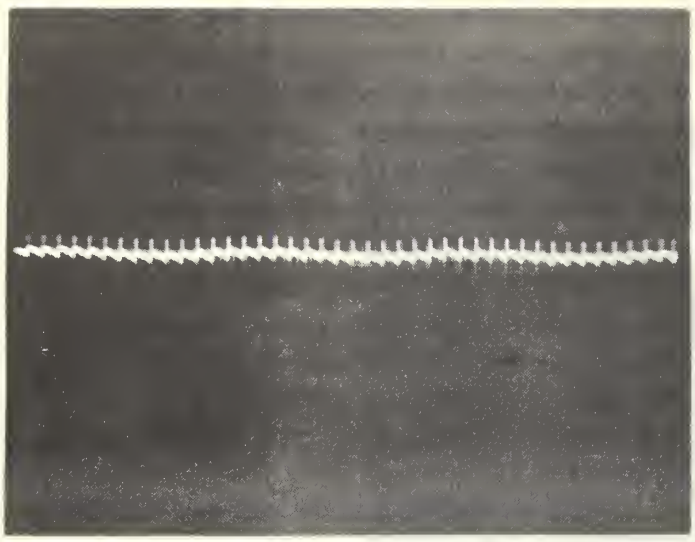


Input sine wave



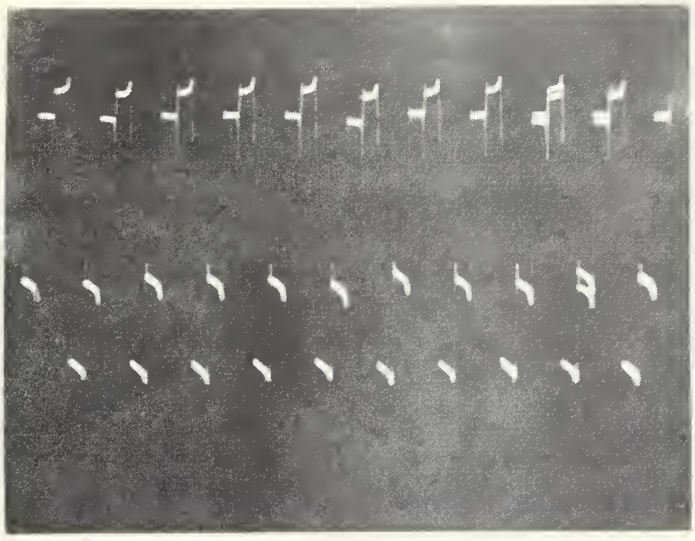
Input sine wave

Output sine wave

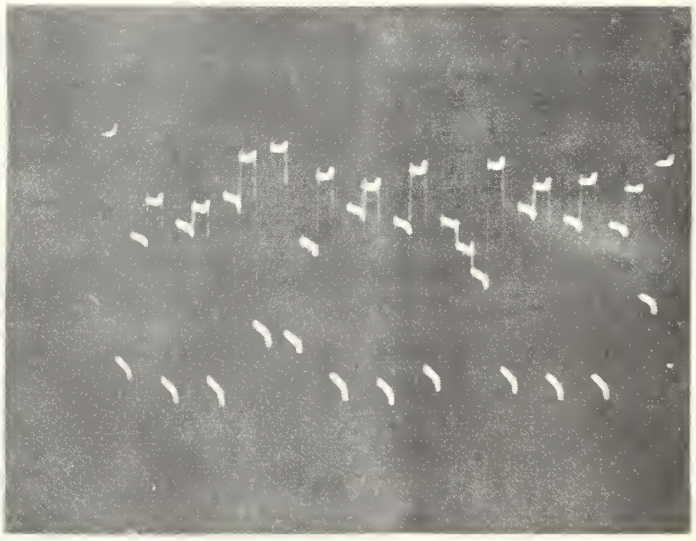
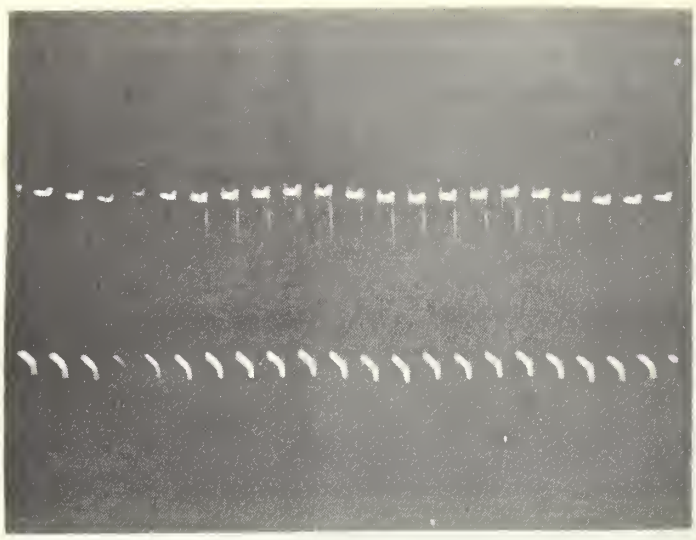


Output at 0 Cps

Output at 100 Cps

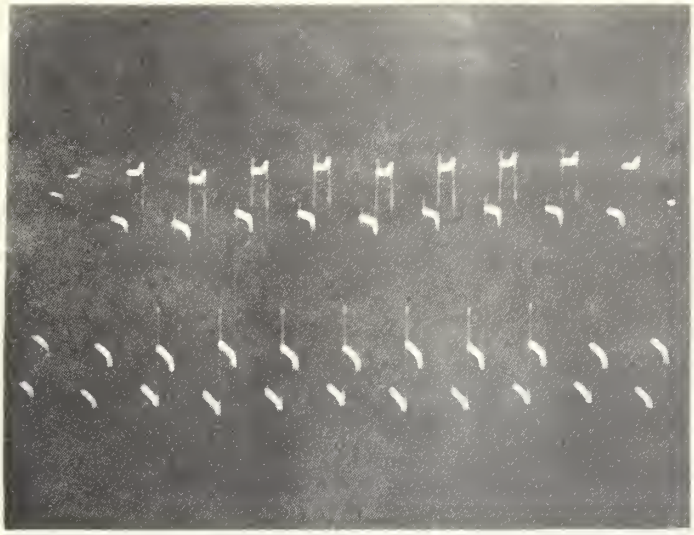


Output at 200 Cps

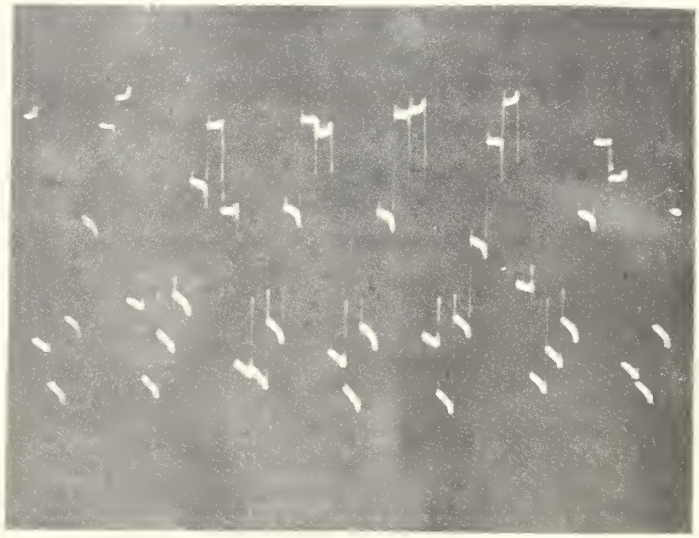
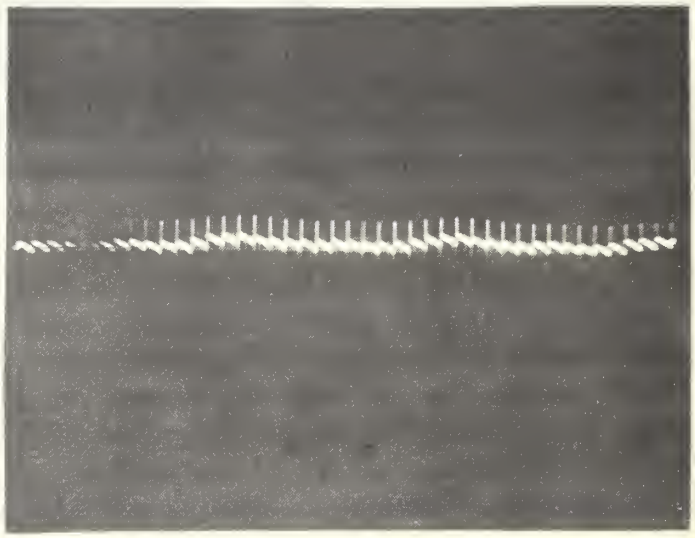
Output at 300 Cps



Output at 400 Cps

Output at 500 Cps



Output at 600 Cps

Output at 700 Cps



Output at 800 Cps

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13. ABSTRACT

By using a series of diode sampling gates and capacitive storage elements to achieve the necessary time delay, a cancellation filter is designed that will give a maximally flat passband and that will give subclutter rejection at zero frequency and at harmonics of the pulse repetition frequency. Such a filter is necessary in each range channel of moving target indication (MTI) radar systems. Theoretical results obtained from digital simulation are compared with actual results obtained upon completion of the filter synthesis, and a brief evaluation of the entire range channel is presented.

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Cancellation Filter						
MTI Radar						

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